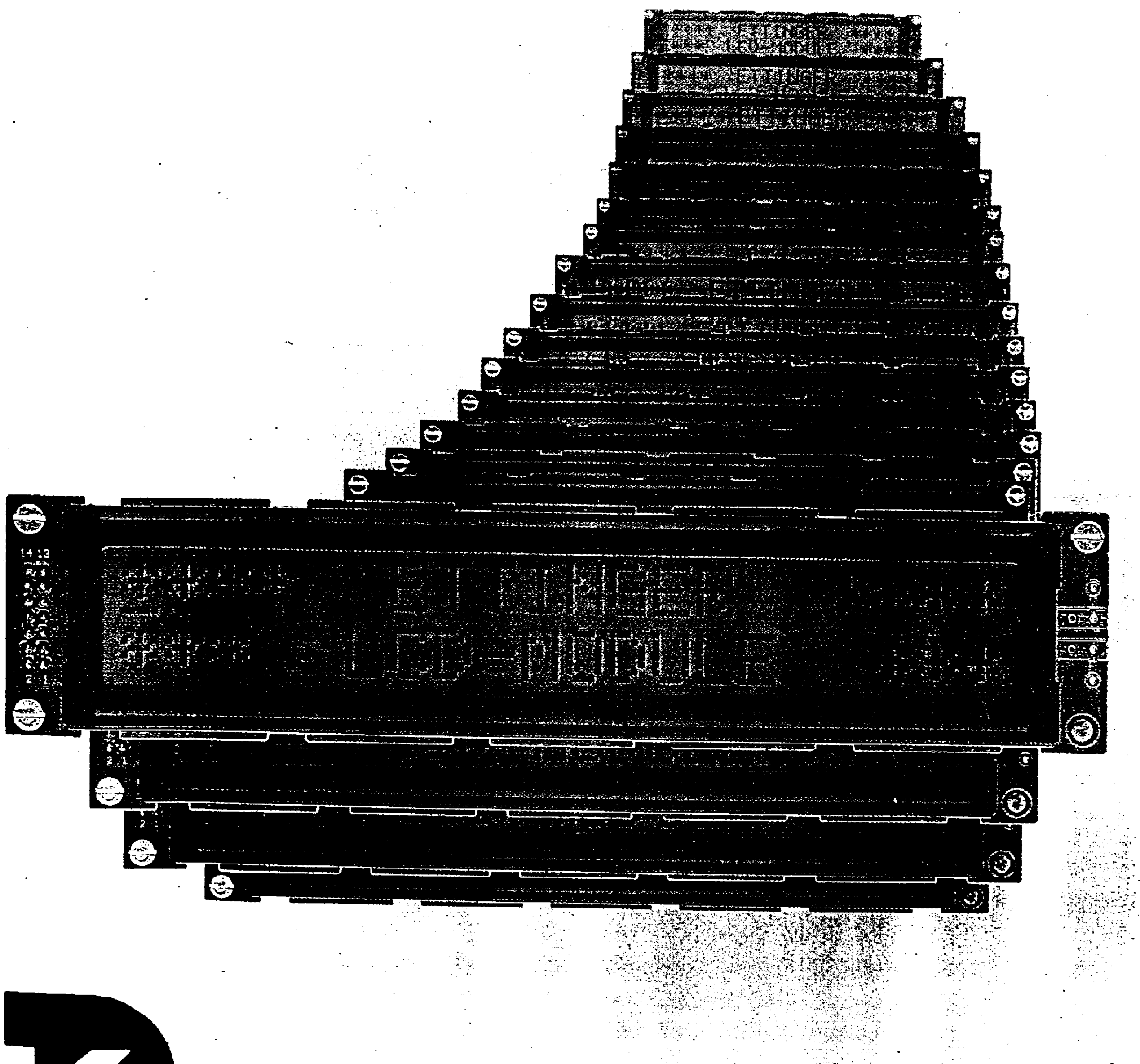
ETTINGER

Elektronik-Bauelemente

... mit Abstand präziser

LCD-MODULE



DATA VISION

LCD-MODULE

DV-16100

16 chars × **1** line **TN/STN** Reflective/EL/LED Backlight *

■ ABSOLUTELY MAXIMUM RATINGS

Item	Symbol	Standard Value			Unit
		Min	Typ.	Max.	
Supply Voltage for Logic	$V_{DD}-V_{SS}$	0	–	7.0	V
Supply Voltage for LCD Driver	$V_{DD}-V_{EE}$	–	–	13.5	V
Input Voltage	V_I	Vss	–	V_{DD}	V
Operature Temp.	Topr	0	–	50	°C
Storage Temp.	Tstg	– 20	–	70	°C

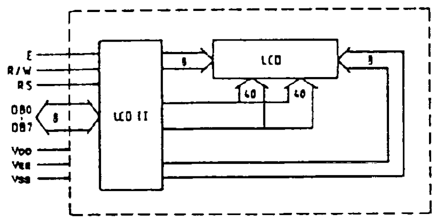
■ ELECTRICAL CHARACTERISTIC (REFLECTIVE TYPE)

Item	Symbol	Test Condition	Standard Value			Unit
			Min.	Typ.	Max.	
Input "High" Voltage	V_{IH}	–	2.2	–	V_{EE}	V
Input "Low" Voltage	V_{IL}	–	–	–	0.6	V
Output "High" Voltage	V_{OH}	I_{OH} = 0.2mA	2.2	–	–	V
Output "Low" Voltage	V_{OL}	I_{OL} = 1.2mA	–	–	0.4	V
Supply Current	I_{DD}	V_{DD} = 5.0A	–	1.0	3.0	mA

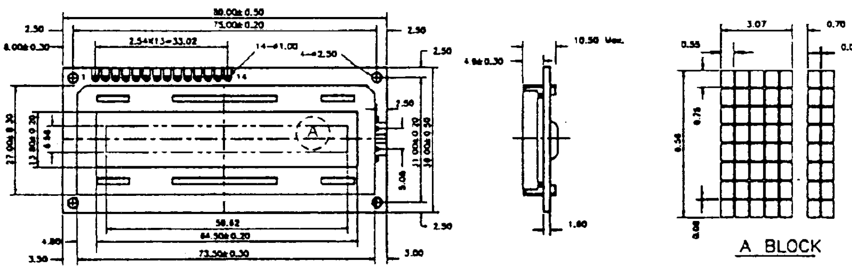
■ PIN FUNCTIONS

No	Symbol	Function	No	Symbol	Function
1	Vss	GND, 0V	8	DB1	Data Bus
2	VDD	+5V	9	DB2	–
3	VEE	for LCD Drive	10	DB3	–
4	RS	Function Select	11	DB4	–
5	R/W	Read/Write	12	DB5	–
6	E	Enable Signal	13	DB6	–
7	DB0	Data Bus Line	14	DB7	–

■ BLOCK DIAGRAM



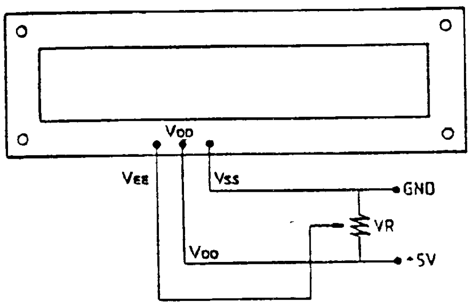
■ DIMENSION OUTLINE



A BLOCK

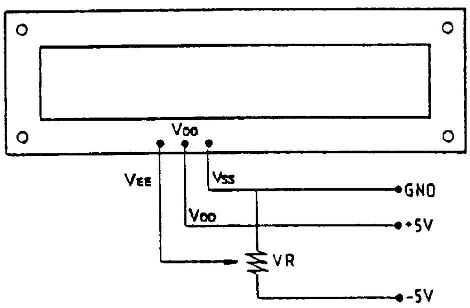
* Anschluß LED-Version: 7,5 Ohm an Anode (+ 5V), Kathode (0V)

For Single Power (Normal Temp Type)



VR : 10K - 20KΩ

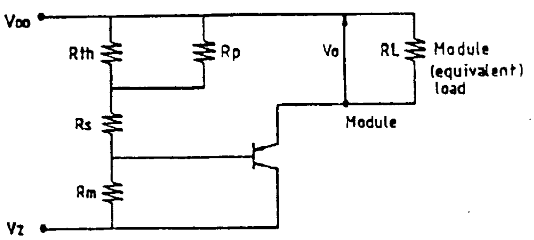
For Dual Power (Extended Temp Type)

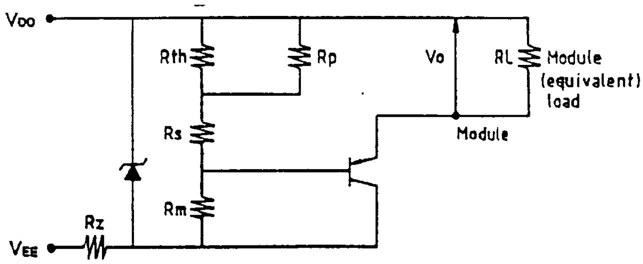


VR : 10K - 20KΩ

Examples of Temperature Compensation Circuits For Extended Temperature LCM. (Reference Data)

Figure 1. (1/16 Duty, 1/4 Bias)





Befehlssatz

Adresse / Befehl	RS	R/W	D7	D6	D5	D4	D3	D2	D1	D0
Display clear	0	0	0	0	0	0	0	0	0	1
Cursor home	0	0	0	0	0	0	0	0	1	·
Entry mode set	0	0	0	0	0	0	0	1	I/D	S
Display ein/aus	0	0	0	0	0	0	1	D	C	B
Cursor Display shift	0	0	0	0	0	1	S/C	R/L	·	·
Funtion set	0	0	0	0	1	DL	1	0	·	·
CG RAM address set	0	0	0	1	A_{CG}					
DD RAM address set	0	0	1	A_{DD}						
Busy flag lesen	0	1	BF							
CG RAM/DD RAM Daten schreiben	1	0	Daten schreiben							
CG RAM/DD RAM Daten lesen	1	1	Daten lesen							

Anmerkung:

I/D = 1: increment	I/D = 0: decrement
S = 1: Display shift	S = 0: Display freeze
D = 1: Display an	D = 0: Display aus
C = 1: Cusor an	C = 0: Cursor aus
B = 1: Zeichen in Cursorposition blinkt	
S/C = 1: Display shift	S/C = 0: Cursor weiter
R/L = 1: shift rechts	R/L = 0: shift linlks
DL = 1: 8-Bitbus	DL = 0: 4-Bitbus
BF = 1: Abarbeitung intern	BF = 0: eingabebereit

Zeichensatz

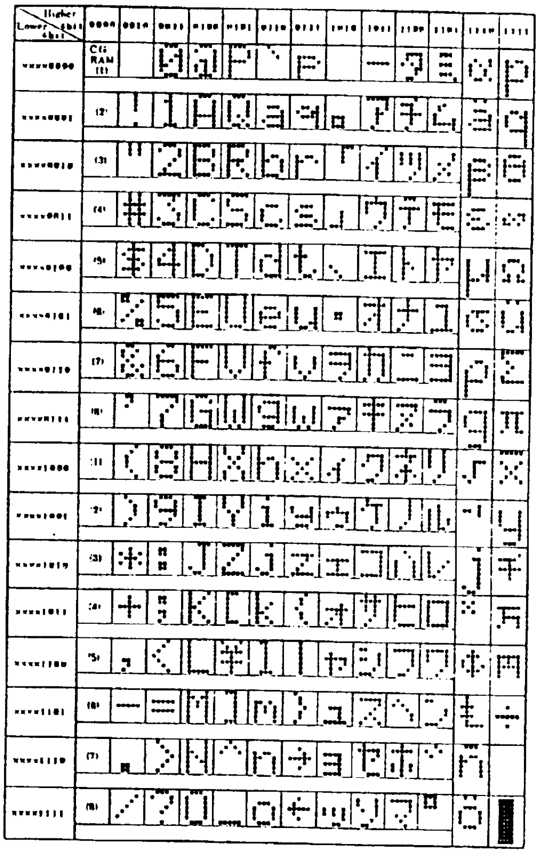
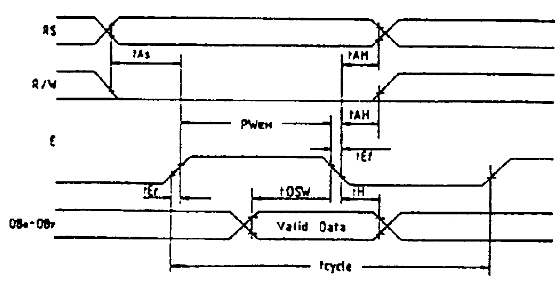
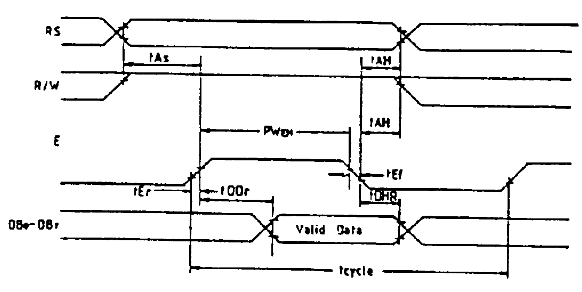


Fig. 1 WRITE OPERATION



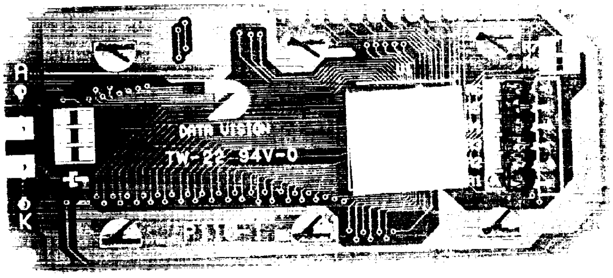
Write data from MPU to LCM

Fig. 2 READ OPERATION



Read data from LCM to MPU

183261



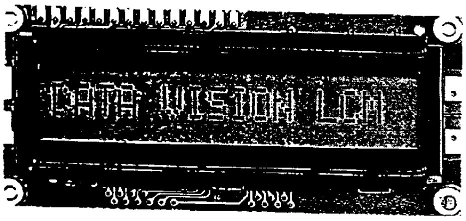
Character LCM/DV series

Display Format char. x line	Model No.	Character Fonts	Module Size (W x H x Tmm)	View Area (W x Hmm)	Character Size (W x Hmm)	Dot Size (W x Hmm)	Po[illegible]r VDD – (V
16 x 1	DV-16100	5 x 8 dots	80.0 x 36.0 x 10.0	64.5 x 13.8	3.07 x 6.56	0.55 x 0.75	0
	DV-16102	5 x 8 dots	85.0 x 36.0 x 13.5	63.5 x 15.8	3.20 x 5.55	0.60 x 0.75	5.0
	DV-16110	5 x 7 dots + Cursor	122.0 x 33.0 x 10.0	99.0 x 13.0	4.84 x 8.06	0.92 x 1.10	5.0
16 x 2	DV-16210	5 x 7 dots + Cursor	122.0 x 44.0 x 10.0	99.0 x 24.0	4.84 x 8.06	0.92 x 1.10	0
	DV-16230	5 x 8 dots	85.0 x 29.5 x 10.0	62.5 x 16.1	2.78 x 4.89	0.55 x 0.50	5.0
	DV-16235	5 x 8 dots	85.0 x 35.0 x 10.0	62.2 x 17.9	2.95 x 5.55	0.55 x 0.65	*5.0
	DV-16236	5 x 8 dots	85.5 x 36.0 x 10.0	62.2 x 17.9	2.95 x 5.55	0.55 x 0.65	0
	DV-16244	5 x 8 dots	84.0 x 44.0 x 10.0	62.2 x 17.9	2.95 x 5.55	0.55 x 0.65	.0
	DV-16252	5 x 8 dots	80.0 x 36.0 x 10.0	62.5 x 16.1	2.78 x 4.89	0.55 x 0.50	5.0
16 x 4	DV-16400	5 x 8 dots	87.0 x 60.0 x 10.0	61.4 x 25.0	2.95 x 4.75	0.55 x 0.55	0
20 x 2	DV-20200	5 x 8 dots	116.0 x 36.0 x 10.0	83.0 x 18.8	3.20 x 5.55	0.60 x 0.65	.0
	DV-20210	5 x 7 dots + Cursor	180.0 x 40.0 x 10.0	149.0 x 23.0	6.00 x 9.66	1.12 x 1.12	*5.0
	DV-20220	5 x 8 dots	108.0 x 39.0 x 10.0	83.0 x 18.8	3.20 x 5.55	0.60 x 0.65	0
20 x 4	DV-20400	5 x 8 dots	98.0 x 60.0 x 10.0	76.0 x 25.2	2.95 x 4.75	0.55 x 0.55	.0
24 x 2	DV-24200	5 x 8 dots	118.0 x 36.0 x 10.0	94.5 x 18.0	3.20 x 5.55	0.60 x 0.65	5.0
	DV-24210	5 x 7 dots + Cursor	208.0 x 40.0 x 10.0	178.0 x 23.0	6.00 x 9.66	1.12 x 1.12	0
40 x 2	DV-40200	5 x 8 dots	182.0 x 33.5 x 10.0	154.0 x 16.5	3.20 x 5.55	0.60 x 0.65	0
40 x 4	DV-40400	5 x 8 dots	190.0 x 54.0 x 10.5	147.0 x 29.5	3.54 x 4.89	0.50 x 0.55	*5.0

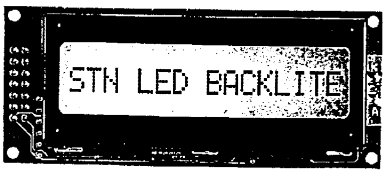
Note * Except for extended temperature LCD.

** TN - Twist nematic STN - Supper twist nematic H - Extended temperature

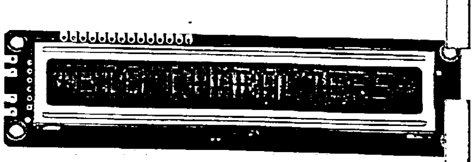
R - Reflective type EL - with EL backlight LED - with LED backlight



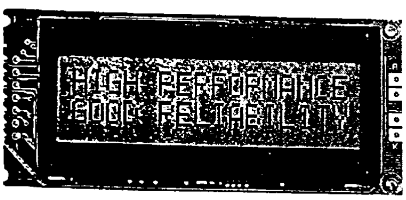
DV-16100



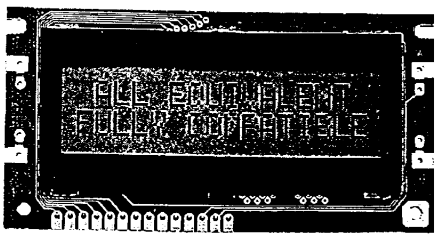
DV-16102



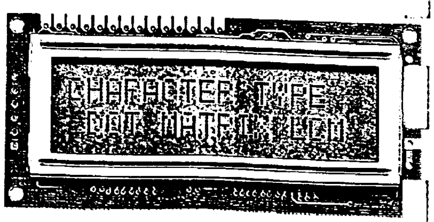
DV-16110



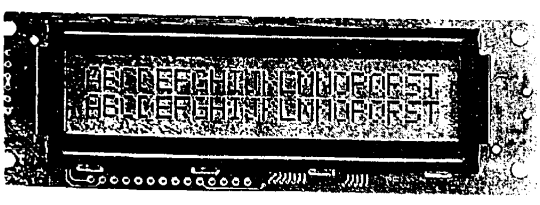
DV-16236



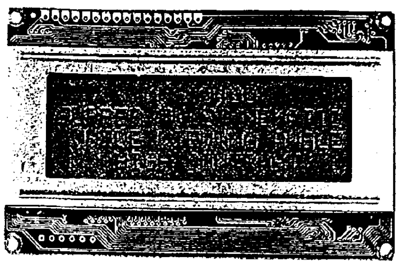
DV-16244



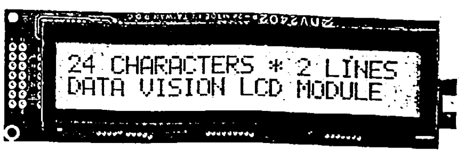
DV-16252



DV-20220

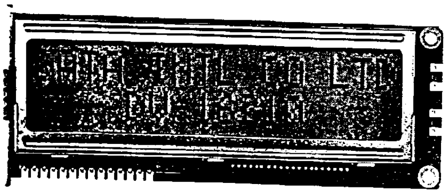


DV-20400

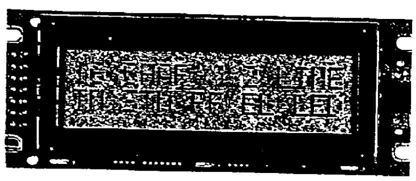


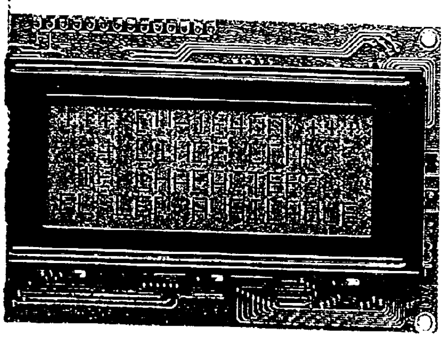
DV-24200

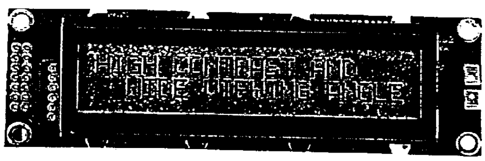
ly ss	Current Consumption typ. (mW)	Built-in Control LSI	Driving Method Duty/Bias	Versions ••						Page	Model No
				TN	STN	H	R	EL	LED		
	10	HD44780 or Equivalent	1/16D,1/4B	o	o		o	o	o	13	DV-16100
	10	HD44780 or Equivalent	1/16D,1/4B		o				o	13	DV-16102
	10	HD44780 or Equivalent	1/16D,1/4B		o		o	o	o	14	DV-16110
	10	HD44780 or Equivalent	1/16D,1/4B	o	o		o	o	o	14	DV-16210
	10	HD44780 or Equivalent	1/16D,1/4B	o	o		o	o	o	15	DV-16230
	10	HD44780 or Equivalent	1/16D,1/4B	o	o	o	o	o	o	15	DV-16235
	10	HD44780 or Equivalent	1/16D,1/4B	o	o	o	o	o	o	16	DV-16236
	10	HD44780 or Equivalent	1/16D,1/4B	o	o	o	o	o	o	16	DV-16244
	10	HD44780 or Equivalent	1/16D,1/4B	o	o		o	o	o	17	DV-16252
	20	HD44780 or Equivalent	1/16D,1/4B	o	o		o	o	o	17	DV-16400
	15	HD44780 or Equivalent	1/16D,1/4B	o	o	o	o	o	o	18	DV-20200
	15	HD44780 or Equivalent	1/16D,1/4B		o	o	o	o	o	18	DV-20210
	15	HD44780 or Equivalent	1/16D,1/4B	o		o	o	o	o	19	DV-20220
	25	HD44780 or Equivalent	1/16D,1/4B		o		o	o	o	19	DV-20400
	20	HD44780 or Equivalent	1/16D,1/4B	o	o		o	o	o	20	DV-24200
	20	HD44780 or Equivalent	1/16D,1/4B		o		o			20	DV-24210
	25	HD44780 or Equivalent	1/16D,1/4B		o	o	o	o	o	21	DV-40200
	50	HD44780 or Equivalent	1/16D,1/4B		o	o	o	o	o	21	DV-40400

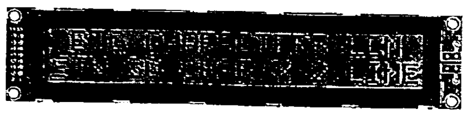

DV-16210


DV-16230


DV-16235

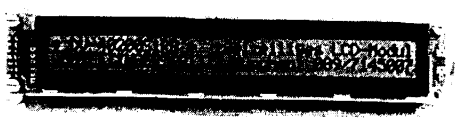

DV-16400

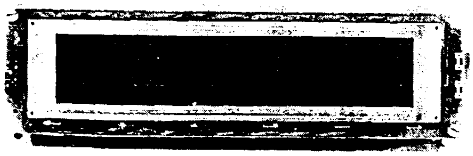

DV-20200


DV-20210



DV-24210

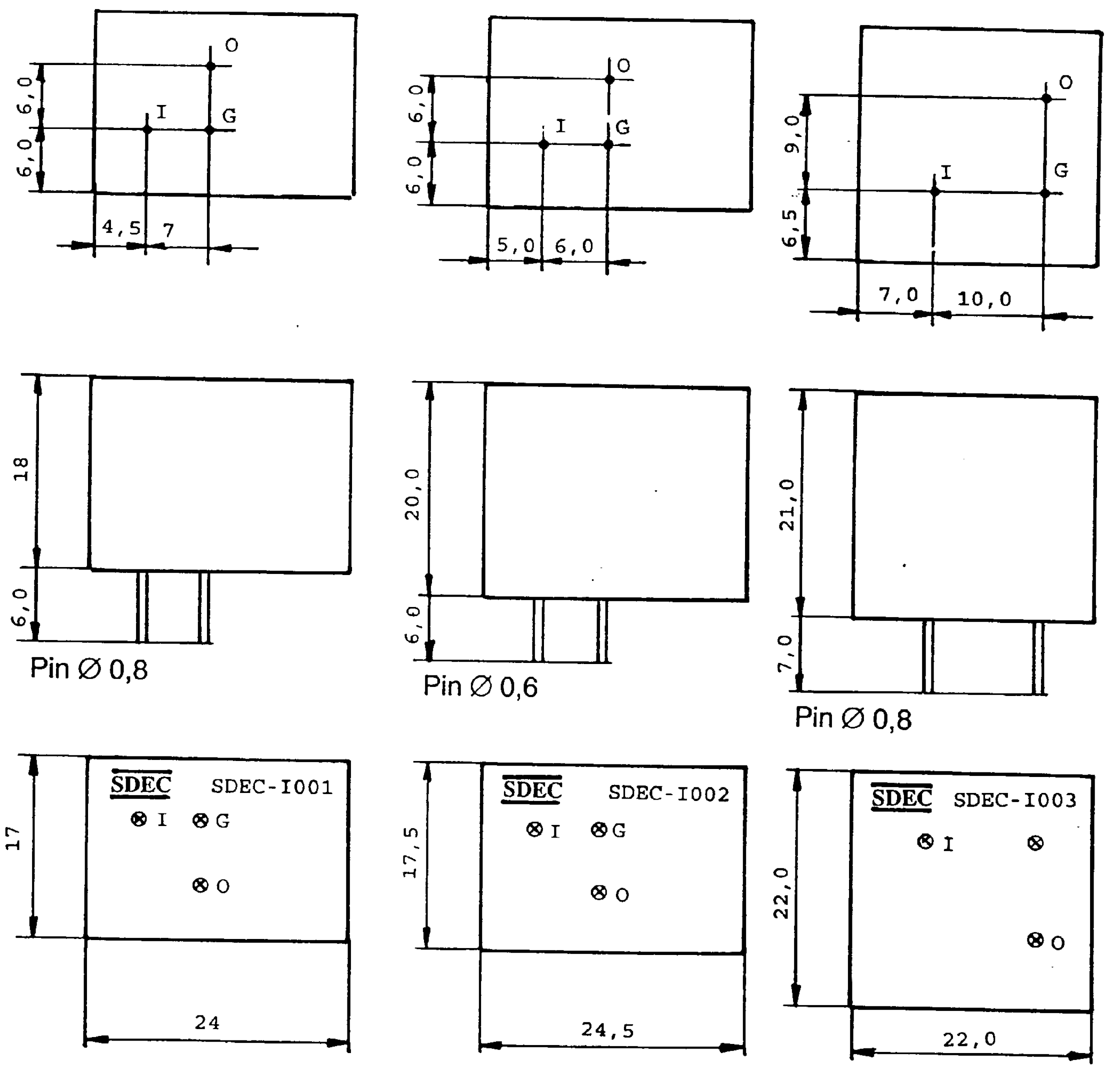

DV-40200


DV-40400

Inverter für EL

Passend für transflektive Versionen mit Elektrolumineszenzfolie

	SDEC-I001	SDEC-I002	SDEC-I003	
U ein	4,5 - 6,5	5 +/- 5%	5 +/- 5%	V
U aus	100	90 - 110	90 - 110	V
I ein	25	45	65	mA
F inv.	400 - 580	400 - 660	400 - 600	Hz
Akt.EL-Fläche	9 - 15	17 - 31	45 - 55	cm2



Arbeitstemperaturbereich: − 10° ... + 60° Celsius
Lagertemperaturbereich: − 20° ... + 70° Celsius

PIN	O	G	I
Funktion	Ausgang für EL-Folie	Gnd / EL-Folie	Eingang: 5 V DC

ETTINGER

HOW TO USE HITACHI'S BUILT-IN CONTROLLER DRIVER LCD-II (HD44780) DOT MATRIX LCD MODULE

▪ INTRODUCTION

The LCD-II (HD44780) is a dot matrix liquid crystal display controller & driver LSI that displays alphanumerics, kana characters and symbols. It drives dot matrix liquid crystal display under 4-bit or 8-bit microcomputer or microprocessor control. All the functions required for dot matrix liquid crystal display drive are internally provided on one chip.
The user can complete dot matrix liquid crystal display systems with less number of chips by using the LCD-II (HD44780). If a driver LSI HD44100H is externally connected to the HD44780, up to 80 characters can be displayed.
The LCD-II is produced in the CMOS process. Therefore, the combination of the LCD-II with a CMOS microcomputer or microprocessor can accomplish a portable battery-drive device with lower power dissipation.

▪ FEATURES

- Capable of interfacing to 4-bit or 8-bit MPU.
- Display data RAM .... 80 x 8 bits
  (80 characters, max.)
- Character generator ROM ....
  Character font 5 x 7 dots: 160 characters
  Character font 5 x 10 dots: 32 characters
- Both display data and character generator RAMs can be read from the MPU.
- Wide range of instruction functions
  Display clear, Cursor home, Display ON/OFF, Cursor ON/OFF, Display character blink, Cursor shift, Display shift
- Internal automatic reset circuit at power ON. (Internal reset circuit)

1. Applicable type

(1) 1 line series

(2) 2 line series

(3) 4 line series

2. Connecting MPU with LCM.

2.1 Driver circuit block diagram

Figure 1 shows the driver circuit block diagram of LCM with built-in controller LSI. Controller LSI HD44780 (LCD-II) is built-in this LCM. Also extended LCD driver LSI is built in the LCM that displays more than 16 digits.

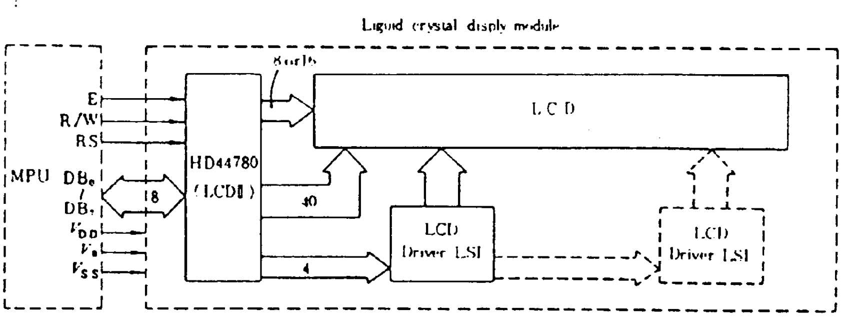


Fig. 1 Driver circuit block diagram

2.2 Interfacing to MPU

In the HD44780, data can be sent in either 4-bit 2-operation or 8-bit 1-operation so it can interface to both 4 and 8 bit MPU's.

(1) When interface data is 4-bits long, data is transferred using only 4 buses: $DB_4 \sim DB_7$. $DB_0 \sim DB_3$ are not used. Data transfer between the HD44780 and the MPU completes when 4-bit data is transferred twice. Data of the higher order 4 bits (contents of $DB_4 \sim DB_7$ when interface data is 8 bits long) is transferred first, then the lower order 4 bits (content of $DB_0 \sim DB_3$ when interface data is 8 bits long) is transferred. Check the busy flag after 4-bit data has been transferred twice (one instruction). A 4-bit 2-operation will then transfer the busy flag and address counter data.

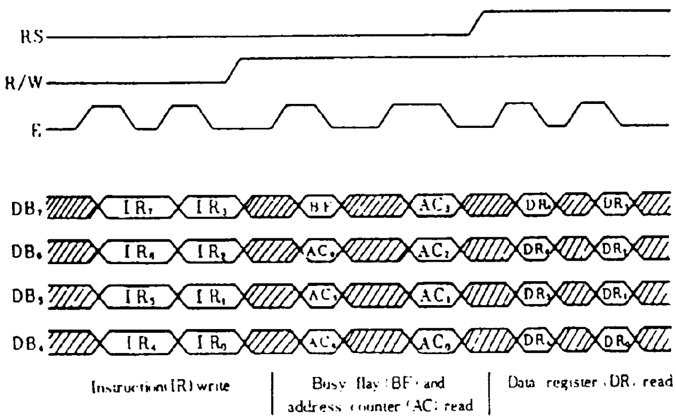


Fig. 2 4-bit data transfer example

(2) When interface data is 8 bit long, data is transferred using the 8 data buses of $DB_0 \sim DB_7$.

2.3 Interface to MPU

(1) Interface to 8-bit MPU

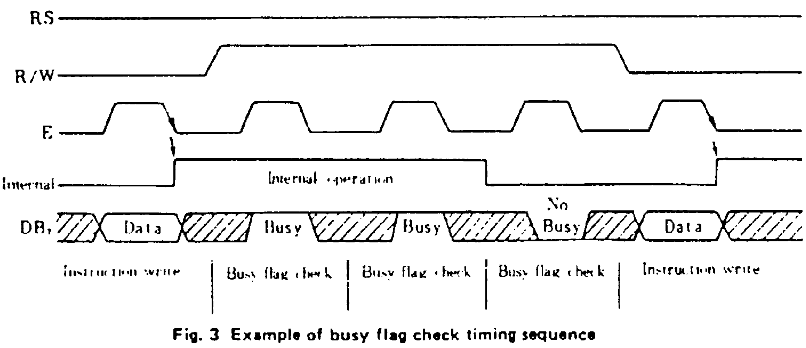


Fig. 3 Example of busy flag check timing sequence

① When connecting to 8-bit MPU through PIA

Fig. 4 is an example of using a PIA or I/O port (for single chip microcomputer) as an interface device. Input and output of the device is TTL compatible.

In the example, PB_0 to PB_7 are connected to the data buses DB_0 to DB_7 and PA_0 to PA_2 are connected to E, R/W and RS respectively. Pay attention to the timing relation between E and other signals when reading or writing data and using PIA as an interface.

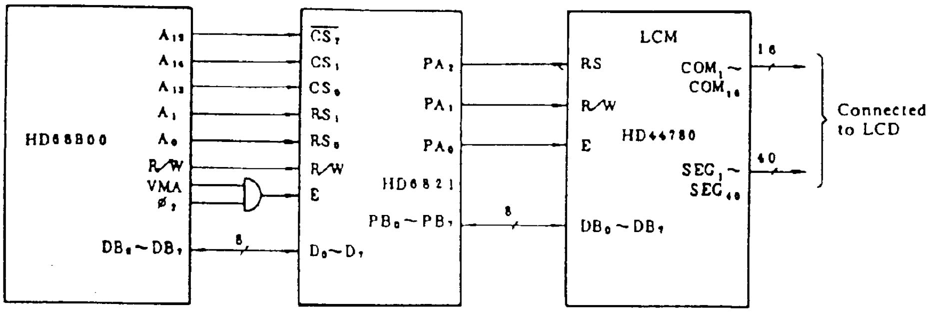
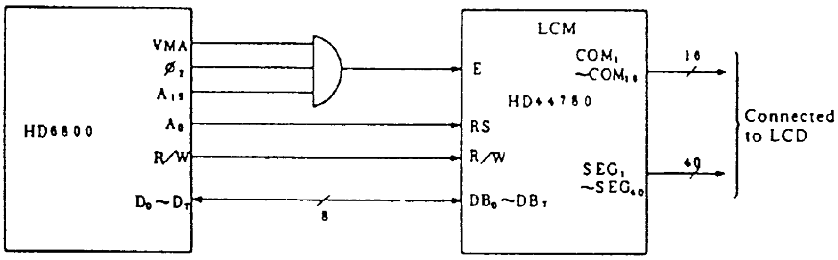
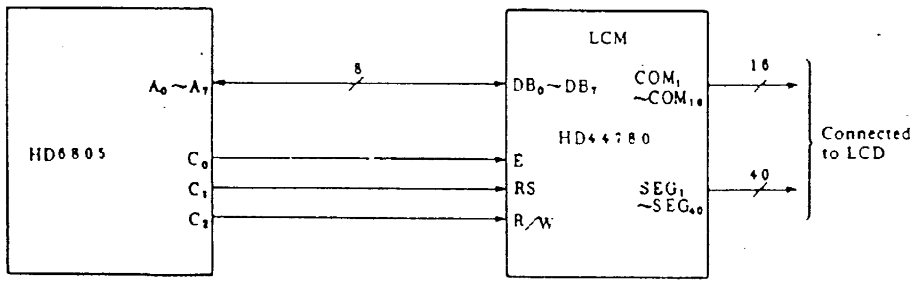


Fig. 4 Example of interface to HD68B00 using PIA (HD68B21)

② Connecting directly to the 8 bit MPU bus line



③ Example of interfacing to the HD6805



④ Example of interfacing to the HD6301

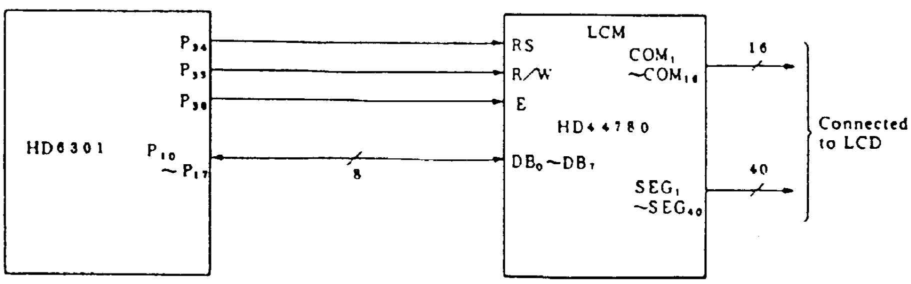


Table 4 Register selection

RS	R W	E	Operation
0	0		IR write as internal operation (Display clear, etc.)
0	1		Read busy flag (DB_7) and address counter (DB_0 ~ DB_6)
1	0		DR write as internal operation (DR to DD or CG RAM)
1	1		DR read as internal operation (DD or CG RAM to DR)

(2) Busy flag (BF)
When the busy flag is "1", the HD44780 is in the internal operation mode, and the next instruction will not be accepted. As Table 4 shows, the busy flag is output to DB_7 when RS = 0 and R/W = 1. The next instruction must be written after ensuring that the busy flag is "0".

(3) Address counter (AC)
The address counter (AC) assigns addresses to DD and CG RAMs. When an instruction for address is written in IR, the address information is sent from IR to AC. Selection of either DD or CG RAM is also determined concurrently by the instruction.
After writing into (or reading from) DD or CG RAM display data, AC is automatically incremented by +1 (or decremented by −1). AC contents are output DB_0 ~ DB_6 when RS = 0 and R/W = 1, as shown in Table 4.

(4) Display data RAM (DD RAM)
The display data RAM (DD RAM) stores display data represented in 8-bit character codes. Its capacity is 80 x 8 bits, or 80 characters. The display data RAM (DD RAM) that is not used for display can be used as a general data RAM. Relations between DD RAM addresses and positions on the liquid crystal display are shown below.
The DD RAM address (A_{DD}) is set in the Address Counter (AC) and is represented in hexadecimal.

	Higher order bits			Lower order bits			
AC	AC6	AC5	AC4	AC3	AC2	AC1	AC0
	Hexadecimal			Hexadecimal			

(Ex.) DD RAM address "4E"

1	0	0	1	1	1	0
4			E			

1-line display (N = 0)

	1	2	3	4	5					79	80	← display position
1-line	00	01	02	03	04					4E	4F	← DD RAM address

(a) When the display characters are less than 80, the display begins at the head position. For example, 8 characters using one HD44780 are displayed as:

	1	2	3	4	5	6	7	8	← display position
1-line	00	01	02	03	04	05	06	07	← DD RAM address

When the display shift operation is performed, the DD RAM address moves as:

01	02	03	04	05	06	07	08	(Left shift display)
4F	00	01	02	03	04	05	06	(Right shift display)

(b) 16-character display using an HD44780 and an HD44100H is as shown below:

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	← display position
1-line	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	← DD RAM address

HD44780 display (positions 1–8) — HD44100H display (positions 9–16)

When the display shift operation is performed, the DD RAM address moves as:

01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	(Left shift display)
4F	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	(Right shift display)

(c) The relation between display position and DD RAM address when the number of display digits is increased through the use of one HD44780 and two or more HD44100H's can be considered an extension of (b).

Since the increase can be 8 digits for each additional HD44100H, up to 80 digits can be displayed by externally connecting 9 HD44100H's.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20		73	74	75	76	77	78	79	80	← display position
1-line	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13		48	49	4A	4B	4C	4D	4E	4F	← DD RAM address

HD44780 display — HD44100H (1) display — HD44100H (2) ~ (8) display — HD44100H (9) display

2-line display (N = 1)

	1	2	3	4	5	...	39	40	← display position
1-line	00	01	02	03	04	....	26	27	← DD RAM address
2-line	40	41	42	43	44	....	66	67	

(a) When the number of display characters is less than 40 x 2 lines, the 2 lines from the head are displayed. Note that the first line end address and the second line start address are not consecutive. For example, when an HD44780 is used, 8 characters x 2 lines are displayed as:

	1	2	3	4	5	6	7	8	← display position
1-line	00	01	02	03	04	05	06	07	← DD RAM address
2-line	40	41	42	43	44	45	46	47	

When display shift is performed, the DD RAM address move as:

01	02	03	04	05	06	07	08	(Left shift display)
41	42	43	44	45	46	47	48	

27	00	01	02	03	04	05	06	(Right shift display)
67	40	41	42	43	44	45	46	

(b) 16 character x 2 line are displayed when an HD44780 and an HD44100H are used.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	← display position
1-line	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	← DD RAM address
2-line	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	

HD44780 display (positions 1–8) — HD44100H display (positions 9–16)

When display shift is performed, the DD RAM address moves as follows:

01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10
41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50

(Left shift display)

27	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E
67	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E

(Right shift display)

(c) The relation between display position and DD RAM address when the number of display digits is increased by using one HD44780 and two or more HD44100H's, can be considered an extension of (b).

Since the increase can be 8 digits x 2 lines for each additional HD44100H, up to 40 digits x 2 lines can be displayed by connecting 4 HD44780's externally.

← display position	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20		33	34	35	36	37	38	39	40
1-line (← DD RAM address)	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	....	20	21	22	23	24	25	26	27
2-line	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50	51	52	53	....	60	61	62	63	64	65	66	67

— HD44780 display — — HD44100 (1) display — — HD44100H (2) (3) display — — HD44100H (4) —

(d) Display position and DD RAM address for

Character NO.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
DD RAM address	00	01	02	03	04	05	06	07	40	41	42	43	44	45	46	47

(Note)Shift display is as same as that of 8 char. × 2 line type.

(e) Display position and DD RAM address for

← display position	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
1-line (← DD RAM address)	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F
2-line	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F
3 line	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F
4-line	50	51	52	53	54	55	56	57	58	59	5A	5B	5C	5D	5E	5F

(f) Display position and DD RAM address for

← display position	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
1-line (← DD RAM address)	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13
2-line	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50	51	52	53
3-line	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F	20	21	22	23	24	25	26	27
4-line	54	55	56	57	58	59	5A	5B	5C	5D	5E	5F	60	61	62	63	64	65	66	67

(Note)Shift display is as same as 2-line type.

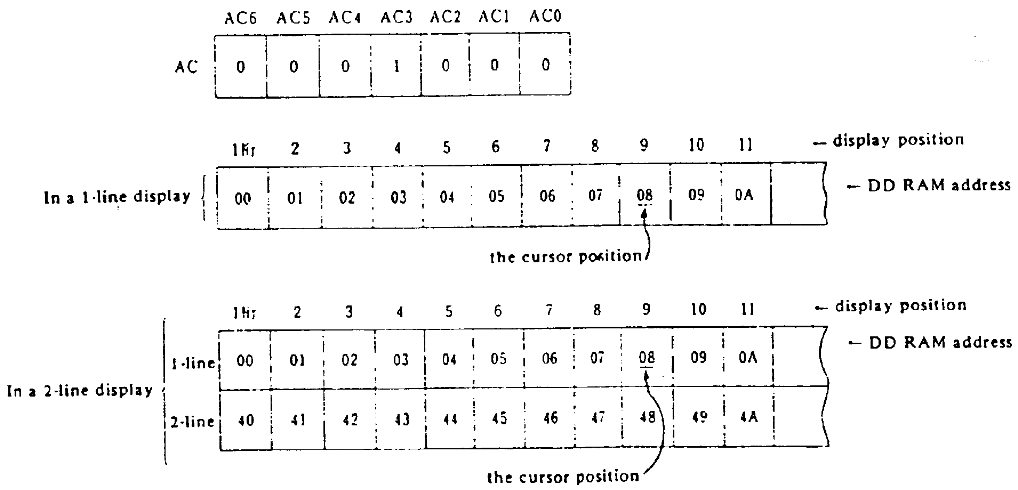
(5) Character generator ROM (CG ROM)
The character generator ROM generates 5 x 7 dot or 5 x 10 dot character patterns from 8-bit character codes. It can generate 160 types of 5 x 7 dot character patterns and 32 types of 5 x 10 dot character patterns. Tables 5(1) and 5(2) show the relation between character codes and character patterns in the Hitachi standard HD44780A00. User defined character patterns are also available by mask-programming ROM. For details, see "The LCD-II (HD44780) Breadboard User's Manual".

(6) Character generator RAM (CG RAM)
The character generator RAM is the RAM with which the user can rewrite character patterns by program. With 5 x 7 dots, 8 types of character patterns can be written and with 5 x 10 dots 4 types can be written. Write the character codes in the left columns of Tables 6(1) and 6(2) to display character patterns stored in CG RAM.
Table 5 shows the relation between CG RAM addresses and data and display patterns.
As Table 5 shows, an area that is not used for display can be used as a general data RAM.

(7) Timing generation circuit
The timing generation circuit generates timing signals to operate internal circuits such as DD RAM, CG ROM and CG RAM. RAM read timing needed for display and internal operation timing by MPU access are separately generated so they do not interfere with each other. Therefore, when writing data to the DD RAM, for example, there will be no undesirable influence, such as flickering, in areas other than the display area. This circuit also generates timing signals to operate the externally connected driver LSI HD44100H.

(8) Liquid crystal display driver circuit
The liquid crystal display driver circuit consists of 16 common signal drivers and 40 segment signal drivers. When character font and number of lines are selected by a program, the required common signal drivers automatically output drive waveforms, the other common signal drivers continue to output non-selection waveforms. The segment signal driver has essentially the same configuration as the driver LSI HD44100H. Character pattern data is sent serially through a 40-bit shift register and latched when all needed data has arrived. The latched data controls the driver for generating drive waveform outputs.
The serial data is sent to the HD44100H, externally connected in cascade, used for display digit number extension. Send of serial data always starts at the display data character pattern corresponding to the last address of the display data RAM (DD RAM). Since serial data is latched when the display data character pattern, corresponding to the starting address, enters the internal shift register, the HD44780 drives the head display. The rest displays, corresponding to latter addresses, are added with each additional HD44100H.

(9) Cursor/Blink control circuit
This is the circuit that generates the cursor or blink. The cursor or the blink appear in the digit residing at the display data RAM (DD RAM) address set in the address counter (AC).
When the address counter is $(08)_{16}$, a cursor position is:



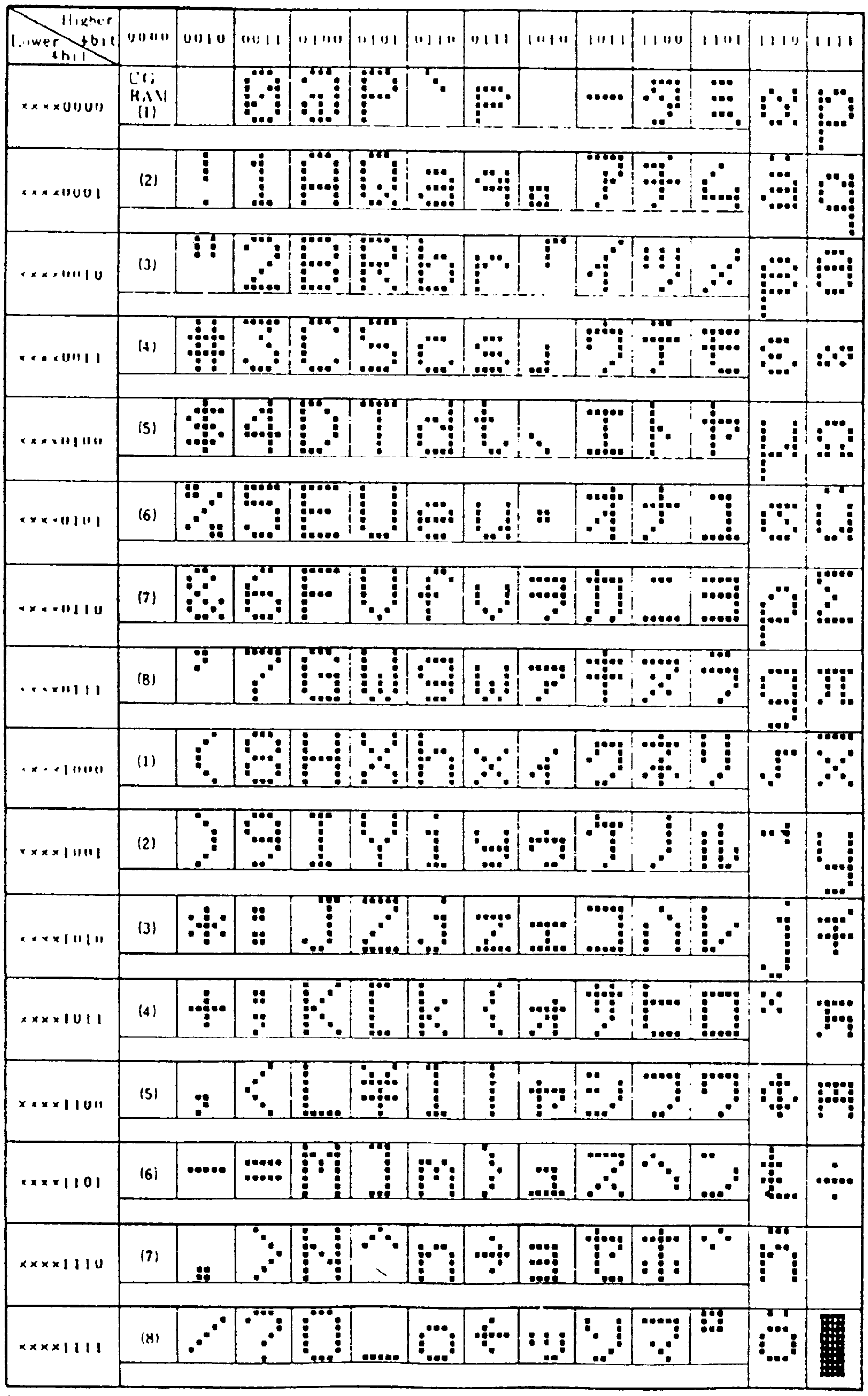
(Note) The cursor or blink appears when the address counter (AC) selects the character generator RAM (CG RAM). But the cursor and blink are meaningless.
The cursor or blink is displayed in the meaningless position when AC is the CG RAM address.

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Table 5

CORRESPONDENCE BETWEEN CHARACTER CODES AND CHARACTER PATTERN

(1) 5 x 10 dot, applied type: H2570, H2571, H2572, LM027, LM067



Note 1. CG RAM is a character generator RAM having a storage function of character pattern which enable to change freely by users program.
Note 2. When line setting at initialization is 2 lines (N = 1), pattern becomes 5 x 7 dot.

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(2) 5 x 7 dot, applied type: Character display modules (including LED backlight versions)

Lower 4 bit \ Higher 4 bit	0000	0010	0011	0100	0101	0110	0111	1010	1011	1100	1101	1110	1111
xxxx0000	CG RAM (1)		0	@	P	`	p		ー	タ	ミ	α	p
xxxx0001	(2)	!	1	A	Q	a	q	。	ア	チ	ム	ä	q
xxxx0010	(3)	"	2	B	R	b	r	「	イ	ツ	メ	β	θ
xxxx0011	(4)	#	3	C	S	c	s	」	ウ	テ	モ	ε	∞
xxxx0100	(5)	$	4	D	T	d	t	、	エ	ト	ヤ	μ	Ω
xxxx0101	(6)	%	5	E	U	e	u	・	オ	ナ	ユ	σ	ü
xxxx0110	(7)	&	6	F	V	f	v	ヲ	カ	ニ	ヨ	ρ	Σ
xxxx0111	(8)	'	7	G	W	g	w	ァ	キ	ヌ	ラ	g	π
xxxx1000	(1)	(	8	H	X	h	x	ィ	ク	ネ	リ	√	x̄
xxxx1001	(2)	)	9	I	Y	i	y	ゥ	ケ	ノ	ル	⁻¹	y
xxxx1010	(3)	*	:	J	Z	j	z	ェ	コ	ハ	レ	j	千
xxxx1011	(4)	+	;	K	[	k	{	ォ	サ	ヒ	ロ	ˣ	万
xxxx1100	(5)	,	<	L	¥	l	|	ャ	シ	フ	ワ	¢	円
xxxx1101	(6)	-	=	M	]	m	}	ュ	ス	ヘ	ン	£	÷
xxxx1110	(7)	.	>	N	^	n	→	ョ	セ	ホ	゛	ñ	
xxxx1111	(8)	/	?	O	_	o	←	ッ	ソ	マ	゜	ö	█

Note: CG ROM is a character generator RAM having a storage function of character pattern which enable to change freely by users program.

Table 6 Relation between CG RAM addresses and character code (DD RAM) and character pattern (CG RAM data).

(1) For 5 x 7 dot character pattern

Character Codes (DD RAM Data) 7 6 5 4 3 2 1 0 ←Higher Lower→	CG RAM Address 5 4 3 ←Higher	CG RAM Address 2 1 0 Lower→	Character Patterns (CG RAM Data) 7 6 5 ←Higher	Character Patterns (CG RAM Data) 4 3 2 1 0 Lower→	
		0 0 0	× × ×	1 1 1 1 0	
		0 0 1	↑	1 0 0 0 1	
		0 1 0		1 0 0 0 1	
0 0 0 0 × 0 0 0	0 0 0	0 1 1		1 1 1 1 0	Character Pattern Example (1)
		1 0 0		1 0 1 0 0	
		1 0 1		1 0 0 1 0	
		1 1 0	↓	1 0 0 0 1	
		1 1 1	× × ×	0 0 0 0 0	← Cursor Position
		0 0 0	× × ×	1 0 0 0 1	
		0 0 1	↑	0 1 0 1 0	
		0 1 0		1 1 1 1 1	
0 0 0 0 × 0 0 1	0 0 1	0 1 1		0 0 1 0 0	Character Pattern Example (2)
		1 0 0		1 1 1 1 1	
		1 0 1		0 0 1 0 0	
		1 1 0	↓	0 0 1 0 0	
		1 1 1	× × ×	0 0 0 0 0	
		0 0 0	× × ×		
		0 0 1	↑		
...	...	...	...	...	
0 0 0 0 × 1 1 1	1 1 1				
		1 0 0			⋇ No effect
		1 0 1			
		1 1 0	↓		
		1 1 1	× × ×		

(Note) 1: Character code bits 0 ~ 2 correspond to CG RAM address bits 3 ~ 5 (3 bits: 8 types).

2: CG RAM address bits 0 ~ 2 designate character pattern line position. The 8th line is the cursor position and display is performed in logical OR by the cursor.
Maintain the 8th line data, corresponding to the cursor display position, in the "0" state for cursor display. When the 8th line data is "1", bit 1 lights up regardless of cursor existence.

3: Character pattern row positions correspond to CG RAM data bits 0 ~ 4, as shown in the figure (bit 4 being at the left end). Since CG RAM data bits 5 ~ 7 are not used for display, they can be used for the general data RAM.

4: As shown in Tables 3 and 4, CG RAM character patterns are selected when character code bits 4 ~ 7 are all "0". However, since character code bit 3 is a ineffective bit, the "R" display in the character pattern example, is selected by character code "00" (hexadecimal) or "08" (hexadecimal).

5: "1" for CG RAM data corresponds to selection for display and "0" for non-selection.

(2) For 5 x 10 dot character pattern

Character Codes (DD RAM Data)		CG RAM Address		Character Patterns (CG RAM Data)	
7 6 5 4 3 2 1 0 ← Higher Lower →		5 4 3 2 1 0 ← Higher Lower →		7 6 5 4 3 2 1 0 ← Higher Lower →	
		0 0 0 0		× × × 0 0 0 0 0	
		0 0 0 1		↑ 0 0 0 0 0	
		0 0 1 0		1 0 1 1 0	
		0 0 1 1		1 1 0 0 1	Character Pattern Example
		0 1 0 0		1 0 0 0 1	
0 0 0 0 × 0 0 ×		0 0 0 1 0 1		1 0 0 0 1	
		0 1 1 0		1 1 1 1 0	
		0 1 1 1		1 0 0 0 0	
		1 0 0 0		1 0 0 0 0	
		1 0 0 1		↓ 1 0 0 0 0	
		1 0 1 0		× × × 0 0 0 0 0	← Cursor Position
		1 0 1 1		× × × × × × × ×	
		1 1 0 0		↑ ↑	
		1 1 0 1			
		1 1 1 0		↓ ↓	
		1 1 1 1		× × × × × × × ×	
		0 0 0 0		× × ×	
		0 0 0 1		↑	
0 0 0 0 × 1 1 ×		1 1 1 0 0 1		↓	
		1 0 1 0		× × ×	
		1 0 1 1		× × × × × × × ×	
		1 1 0 0		↑ ↑	
		1 1 0 1			✱ No effect
		1 1 1 0		↓ ↓	
		1 1 1 1		× × × × × × × ×	

(Note) 1: Character code bits 1, 2 correspond to CG RAM address bits 4, 5 (2 bits: 4 types).

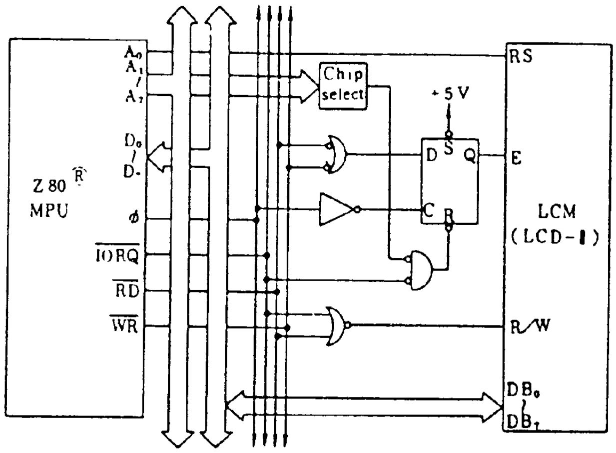
2: CG RAM address bits 0 ~ 3 designate character pattern line position. The 11th line is the cursor position and display is performed in logical OR with cursor.
Maintain the 11th line data corresponding to the cursor display position in the "0" state for cursor display. When the 11th line data is "1", bit 1 lights up regardless of cursor existence. Since the 12th ~ 16th lines are not used for display, they can be used for the general data RAM.

3: Character pattern row positions are the same as 5 x 7 dot character pattern positions.

4: CG RAM character patterns are selected when character code bits 4 ~ 7 are all "0". However, since character code bit 0 and 3 are ineffective bits, "P" display in the character pattern example is selected by character code "00", "01", "08" and "09" (hexadecimal).

5: "1" for CG RAM data corresponds to selection for display and "0" for non-selection.

⑤ Example of interfacing to Z80 MPU



Note: Z80 is the trademark of ZILOG, U.S.A.

(a) Above circuit is an example of connection with Z80 MPU and HD44780A00 as an I/O equipment. It can be used as a part of memories by using MREQ signal.

(b) A0 signal can be used for RS signal.
A0 = 0: Instruction register is selected.
A0 = 1: Data register is selected.

(c) In order to check busy flag, transfer the data of $DB_0 \sim DB_7$ to A register (accumulator) by executing In/Out instruction. After that, busy flag can be easily checked by examining DB_7.

⑥ Example of interfacing to 80 CPU family

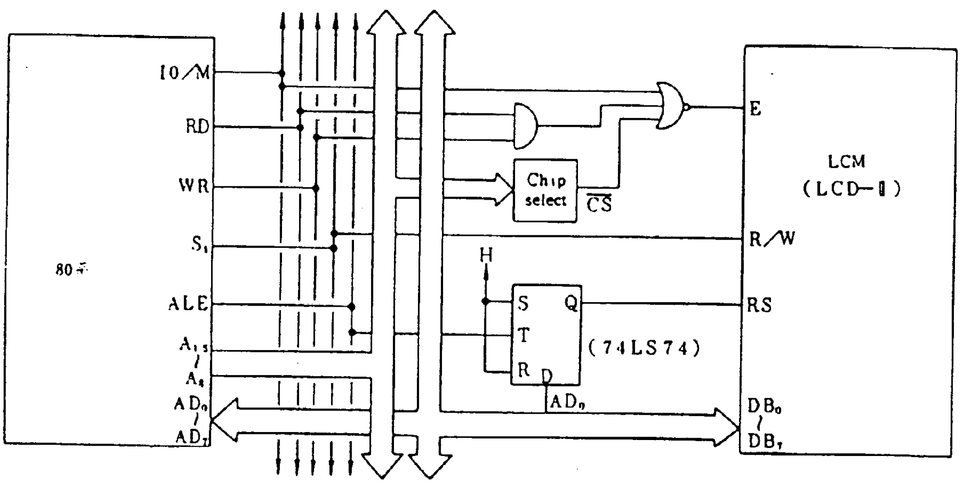


Fig. 5 Example of connection with LCM being used as a part of memories on the determined address.

Figure 5 is an example of connection with LCD module being used as a part of memories on the determined address.

Generates RS signal (Register Select signal) by latching the content of AD_0 at the rising edge of ALE signal. By using this method, you can obtain RS signal from the AD_0 among 8 bit addresses generated at the clock of the first machine cycle. In case of using LCD module as an I/O equipment, chip select signal is necessarily activated when IO/M signal is "High" level.

Furthermore, by using A8 for RS signal, the interface is easily realized.

By both methods, busy flag can be checked by storing status data into A register (Accumulator) and examining the bit 7 by software.

(2) Interface to 4-bit MPU

The HD44780 can be connected to a 4-bit MPU through the 4-bit MPU I/O port. If the I/O port has enough bits, data can be transferred in 8-bit lengths, but if the bits are insufficient, the transfer is made in two operations of 4 bits each (with designation of interface data length for 4 bits). In the latter case, the timing sequence becomes somewhat complex. (See Fig. 6)

Fig. 7 shows an example of interface to the HMCS43C. Note that 2 cycles are needed for the busy flag check as well as the data transfer. 4-bit operation is selected by program.

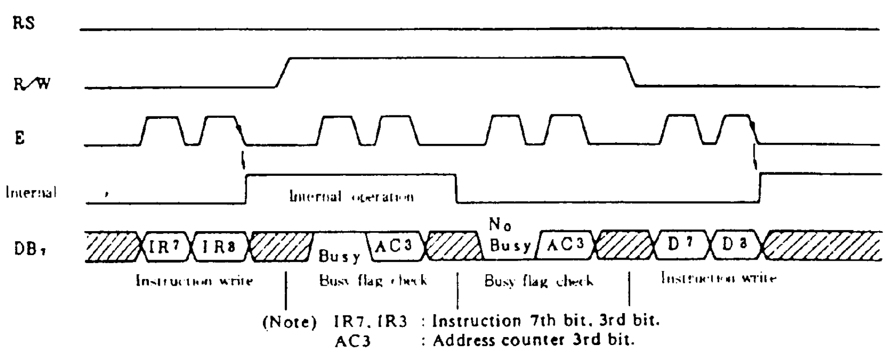


Fig. 6 An example of 4 bit data transfer timing sequence

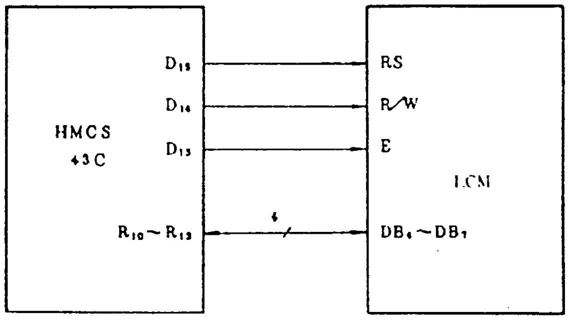


Fig. 7 Example of interface to the HMCS43C

3. Precautions on constituting hardwares

3.1 Chip select

HD44780 has no CS (chip select) terminals. Therefore, when this LSI is connected directly to Data Bus line not through PIA and so on, add the circuit that inhibits the output of Enable signal at the address which is not assigned for HD44780.

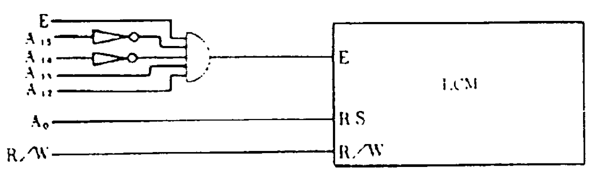


Fig. 8 Example of addresses $(3000)_{16}$ ~ $(3FFF)_{16}$ being assigned for HD44780

3.2 Ability of driving bus line

DB_0 to DB_7 can drive one TTL or capacitance of 130 pF.

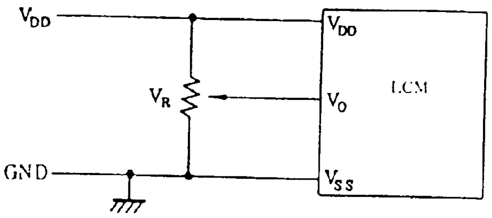
The data bus terminals have three-state constructions and remain in high impedance state while Enable signal being low level.

Since the data bus has pull up MOS, it outputs high level voltage during the data bus being opened.

3.3 Power supply voltage for liquid crystal display drive

At Interface of liquid crystal display module, there are three power supply terminals, V_{DD}, GND, and V_0. LCD module is driven by the voltage that is equal to $V_{DD} - V_0$, when supplying power for liquid crystal display drive to V_0 terminal. Since suitable voltage of power supply for LCD shifts according to temperature change adjust supplying power to LCD by referring to Fig. 9 or Fig. 10.

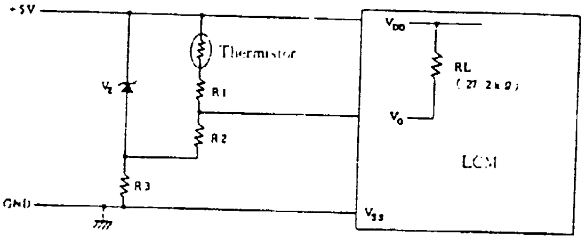
(1) Example of variable driving voltage by a variable resistance (VR)
The driving voltage can be changed by VR to compensate the influence of surrounding temperature.



Recommended VR value = 10kΩ ~ 20kΩ

Fig. 9 Variable driving voltage circuit

(2) Example of a thermal compensator circuit
When setting the voltage, refer to Table-1



Thermistor RT = 15kΩ Ta = 25°C
B = 4.900

Fig. 10 Example of a thermal compensator circuit

Table 1

LCD module	Duty	Recommended driving voltage		Typical circuit parameter			
		Ta (°C)	VDD − VO (V)	VZ (V)	R1 kΩ	R2 kΩ	R3 kΩ
	1/8	0	4.0	4.5	2.2	2.8	1.0
		25	3.7				
		50	3.3				
	1/11	0	4.3	4.5	2.2	3.2	0.3
		25	3.9				
		50	3.3				
	1/16	0	4.6	5.0	0.1	1.3	0.1
		25	4.4				
		50	4.2				

4. Initialization

4.1 Initializing by internal reset circuit

The HD44780 automatically initializes (resets) when power is turned on using the internal reset circuit. The following instructions are executed in initialization. The busy flag (BF) is kept in busy state until initialization ends. (BF = 1) The busy state is 10 ms after V_{CC} rises to 4.5 V.

(1) Display clear
(2) Function set ...... DL = 1 : 8 bit long interface data
N = 0 : 1-line display
F = 0 : 5 x 7 dot character font
(3) Display ON/OFF control .... D = 0 : Display OFF
C = 0 : Cursor OFF
B = 0 : Blink OFF
(4) Entry mode set .... I/D = 1 : +1 (increment)
S = 0 : No shift
(5) Write DD RAM
When the rise time of power supply (0.2 → 4.5) is out of the range 0.1 ms ~ 10 ms, or when the low level width of power OFF (less than 0.2 V) is less than 1 ms, the internal reset circuit will not operate normally.
In this case, initialization will not be performed normally. Initialize by MPU according to "4.2 initializing by instruction" at the head of program.

4.2 Initializing by instruction

If the power supply conditions for correctly operating the internal reset circuit are not met, initialization by instruction is required.

Use the following procedure for initialization.

(1) When interface is 8 bits long;

Power ON

↓

Wait more than 15 ms after V_{DD} rises to 4.5V

↓

RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
0	0	0	0	1	1	x	x	x	x

BF cannot be checked before this instruction.
Function set (interface is 8 bits long)

↓

Wait more than 4.1 ms

↓

RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
0	0	0	0	1	1	x	x	x	x

BF cannot be checked before this instruction.
Function set (interface is 8 bits long)

↓

Wait more than 100 μs

↓

RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
0	0	0	0	1	1	x	x	x	x

BF cannot be checked before this instruction
Function set (interface is 8 bits long)

BF can be checked after the following instructions. When BF is not checked, the waiting time between instructions is longer than the execution instruction time. (See Table 2)

↓

RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0	
0	0	0	0	1	1	N	F	x	x	function set
0	0	0	0	0	0	1	0	0	0	display OFF
0	0	0	0	0	0	0	0	0	1	display ON
0	0	0	0	0	0	0	1	I D	S	entry mode set

Interface is 8 bits long. Specify the number of display lines and character font.

The number of display lines and character font cannot be changed afterwards.

↓

Initialization ends

5. Instruction

5.1 Outline

Only two HD44780 registers, the Instruction Register (IR) and the Data Register (DR) can be directly controlled by the MPU. Prior to internal operation start, control information is temporarily stored in these registers, to allow interface from HD44780 internal operation to various types of MPUs which operate in different speeds or to allow interface to peripheral control ICs. HD44780 internal operation is determined by signals sent from the MPU. These signals include register selection signals (RS), read/write signals (R/W) and data bus signals ($DB_0 \sim DB_7$), and are called instructions, here. Table 2 shows the instructions and their execution time. Details are explained in subsequent sections.

Instructions are of 4 types, those that,

(1) Designate HD44780 functions such as display format, data length, etc.
(2) Give internal RAM addresses.
(3) Perform data transfer with internal RAM
(4) Others

In normal use, category (3) instructions are used most frequently. However, automatic incrementing by +1 (or decrementing by −1) of HD44780 internal RAM addresses after each data write lessens the MPU program load. The display shift is especially able to perform concurrently with display data write, enabling the user to develop systems in minimum time with maximum programming efficiency. For an explanation of the shift function in its relation to display, see 5.3.

When an instruction is executing during internal operation, no instruction other than the busy flag/address read instruction will be executed.

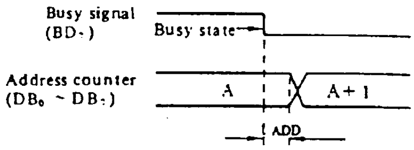
Because the busy flag is set to "1" while an instruction is being executed, check to make sure it is on "1" before sending an instruction from the MPU.

Note 1

Make sure the HD44780 is not in the busy state (BF = 0) before sending the instruction from the MPU to the HD44780. If the instruction is sent without checking the busy flag, the time between first and next instructions is much longer than the instruction time. See Table 2 for a list of each instruction execution time.

Note 2

After executing instruction of writing data to CG/DD RAM or reading data from CG/DD RAM, RAM address counter is automatically incremented by 1 (or decremented by 1). In this case, this shift is executed after Busy Flag is set to "Low". t_{ADD} is stipulated the time from the fall edge of busy flag to the end of address counter's renewal.



t_{ADD} depends on the operating frequency

$$t_{ADD} = \frac{1.5}{f_{CP} \text{ or } f_{osc}} \text{ (s)}$$

(2) When interface is 4 bits long

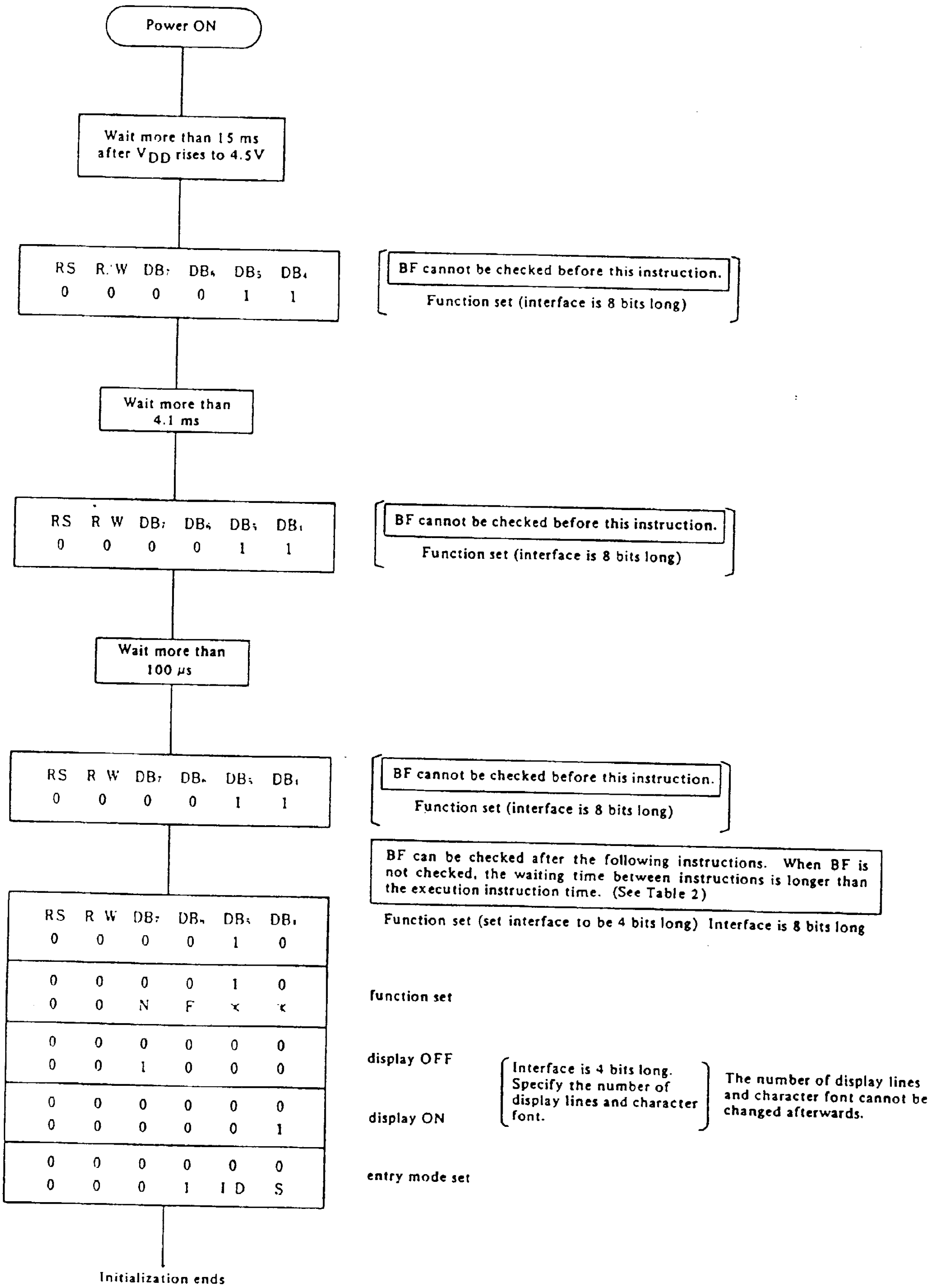


Table 2 Instructions

Instruction	Code										Description	Execution time (when fosc is 250 kHz) Note 1	Execution time (when fosc is 160 kHz) Note 2
	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0			
Clear display	0	0	0	0	0	0	0	0	0	1	Clears all display and returns the cursor to the home position (Address 0).	82 μs ~ 1.64 ms	120 μs ~ 4.9 ms
Return home	0	0	0	0	0	0	0	0	1	*	Returns the cursor to the home position (Address 0). Also returns the display being shifted to the original position. DD RAM contents remain unchanged.	40 μs ~ 1.6 ms	120 μs ~ 4.8 ms
Entry mode set	0	0	0	0	0	0	0	1	I/D	S	Sets the cursor move direction and specifies or not to shift the display. These operations are performed during data write and read.	40 μs	120 μs
Display ON/OFF control	0	0	0	0	0	0	1	D	C	B	Sets ON/OFF of all display (D), cursor ON/OFF (C), and blink of cursor position character (B).	40 μs	120 μs
Cursor and display shift	0	0	0	0	0	1	S/C	R/L	*	*	Moves the cursor and shifts the display without changing DD RAM contents	40 μs	120 μs
Function set	0	0	0	0	1	DL	N	F	*	*	Sets interface data length (DL) number of display lines (L) and character font (F).	40 μs	120 μs
Set CG RAM address	0	0	0	1	A_{CG}						Sets the CG RAM address. CG RAM data is sent and received after this setting.	40 μs	120 μs
Set DD RAM address	0	0	1	A_{DD}							Sets the DD RAM address. DD RAM data is sent and received after this setting.	40 μs	120 μs
Read busy flag & address	0	1	BF	AC							Reads Busy flag (BF) indicating internal operation is being performed and reads address counter contents.	1μs	1 μs
Write data to CG or DD RAM	1	0	Write Data								Writes data into DD RAM or CG RAM.	40 μs	120 μs
Read data to CG or DD RAM	1	1	Read Data								Reads data from DD RAM or CG RAM.	40 μs	120 μs

I/D = 1 Increment (+1) I/D = 0: Decrement (−1)
S = 1 Accompanies display shift.
S/C = 1 Display shift S/C = 0: Cursor move
R/L = 1 Shift to the right.
R/L = 0 Shift to the left.
DL = 1 8 bits DL = 0: 4 bits
N = 1 2 lines N = 0 1 line
F = 1 5 x 10 dots F = 0 5 x 7 dots
BF = 1 Internally operating
BF = 0 Can accept instruction

DD RAM: Display data RAM
CG RAM: Character generator RAM
A_{CG}: CG RAM address
A_{DD}: DD RAM address
Corresponds to cursor address.
AC: Address counter used for both of DD and CG RAM address.

Execution time changes when frequency changes.
(Example)
When fosc is 270 kHz:

$$40\ \mu s \times \frac{250}{270} = 37\ \mu s$$

*No effect
Notes 1. Applied to models driven by 1/8 duty or 1/11 duty.
2. Applied to models driven by 1/16 duty.

5.2 Description of details

(1) Clear display

	RS	R/W	DB_7							DB_0
Code	0	0	0	0	0	0	0	0	0	1

Writes space code "20" (hexadecimal) (character pattern for character code "20" must be blank pattern) into all DD RAM addresses. Sets DD RAM address 0 in address counter. Returns display to its original status if it was shifted. In other words, the display disappears and the cursor or blink go to the left edge of the display (the first line if 2 lines are displayed). Set I/D = 1 (Increment Mode) of Entry Mode. S of Entry Mode doesn't change.

(2) Return home

	RS	R/W	DB_7							DB_0
Code	0	0	0	0	0	0	0	0	0	*

* No effect

Sets the DD RAM address 0 in address counter. Returns display to its original status if it was shifted. DD RAM contents do not change. The cursor or blink go to the left edge of the display (the first line if 2 lines are displayed).

(3) Entry mode set

	RS	R/W	DB_7							DB_0
Code	0	0	0	0	0	0	0	0	I/D	S

I/D: Increments (I/D = 1) or decrements (I/D = 0) the DD RAM address by 1 when a character code is written into or read from the DD RAM. The cursor or blink moves to the right when incremented by 1 and to the left when decremented by 1. The same applies to writing and reading of CG RAM.

S: Shifts the entire display either to the right or to the left when S is 1; to the left when I/D = 1 and to the right when I/D = 0. Thus it looks as if the cursor stands still and the display moves. The display does not shift when reading from the DD RAM when writing into or reading out from the CG RAM does it shift when S = 0.

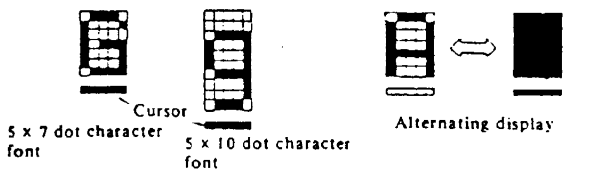
(4) Display ON/OFF control

	RS	R/W	DB_7							DB_0
Code	0	0	0	0	0	0	1	D	C	B

D: The display is ON when D = 1 and OFF when D = 0. When off due to D = 0, display data remains in the DD RAM. It can be displayed immediately by setting D = 1.

C: The cursor displays when C = 1 and does not display when C = 0. Even if the cursor disappears, the function of I/D, etc. does not change during display data write. The cursor is displayed using 5 dots in the 8th line when the 5 x 7 dot character font is selected and 5 dots in the 11th line when the 5 x 10 dot character font is selected.

B: The character indicated by the cursor blinks when B = 1. The blink is displayed by switching between all blank dots and display characters at 409.6 ms interval when f_{CP} or f_{osc} = 250 kHz. The cursor and the blink can be set to display simultaneously. (The blink frequency changes according to the reciprocal of f_{CP} or f_{osc}. $409.6 \times \frac{250}{270} = 379.2$ ms when f_{CP} = 270 kHz.)



(a) Cursor Display Example (b) Blink Display Example

(5) Cursor or display shift

	RS	R/W	DB_7							DB_0
Code	0	0	0	0	0	1	S/C	R/L	*	*

* No effect

Shifts cursor position or display to the right or left without writing or reading display data. This function is used to correct or search for the display. In a 2-line display, the cursor moves to the 2nd line when it passes the 40th digit of the 1st line. Notice that the 1st and 2nd line displays will shift at the same time. When the displayed data is shifted repeatedly each line only moves horizontally. The 2nd line display does not shift into the 1st line position.

S/C	R/L	
0	0	Shifts the cursor position to the left. (AC is decremented by one.)
0	1	Shifts the cursor position to the right. (AC is incremented by one.)
1	0	Shifts the entire display to the left. The cursor follows the display shift.
1	1	Shifts the entire display to the right. The cursor follows the display shift.

Address counter (AC) contents do not change if the only action performed is shift display.

(6) Function set

	RS	R/W	DB_7							DB_0
Code	0	0	0	0	1	DL	N	F	•	•

* No effect

DL: Sets interface data length. Data is sent or received in 8 bit lengths (DB_7 ~ DB_0) when DL = 1 and in 4 bit lengths (DB_7 ~ DB_4) when DL = 0.
When the 4 bit length is selected, data must be sent or received twice.

N: Sets number of display lines.

F: Sets character font.

(Note) Perform the function at the head of the program before executing all instructions (except "Busy flag/address read"). From this point, the function set instruction cannot be executed unless the interface data length is changed.

N F	No. of display lines	Character font	Duty factor	Remarks
0 0	1	5 x 7 dots	1/8	
0 1	1	5 x 10 dots	1/11	
1 •	2	5 x 7 dots	1/16	Cannot display 2 lines with 5 x 10 dot character font.

* No effect

(7) Set CG RAM address

	RS	R/W	DB_7							DB_0
Code	0	0	0	1	A	A	A	A	A	A

← Higher Order Bits   Lower Order Bits →

Sets the CG RAM address into the address counter in binary AAAAAA. Data is then written or read from the MPU for the CG RAM.

(8) Set DD RAM address

	RS	R/W	DB_7							DB_0
Code	0	0	1	A	A	A	A	A	A	A

← Higher Order Bits   lower Order Bits →

Sets the DD RAM address into the address counter in binary AAAAAAA. Data is then written or read from the MPU for the DD RAM.

However, when N = 0 (1-line display), AAAAAAA is "00" ~ "4F" (hexadecimal),
when N = 1 (2-line display), AAAAAAA is "00" ~ "27" (hexadecimal) for the first line, and "40" ~ "67" (hexadecimal) for the second line.

(9) Read busy flag & address

	RS	R/W	DB_7							DB_0
Code	0	1	BF	A	A	A	A	A	A	A

← Higher Order Bits   Lower Order Bits →

Reads the busy flag (BF) that indicates the system is now internally operating by a previously received instruction. BF = 1 indicates that internal operation is in progress. The next instruction will not be accepted until BF is set to "0". Check the BF status before the next wire operation.

At the same time, the value of the address counter expressed in binary AAAAAAA is read out. The address counter is used by both CG and DD RAM addresses, and its value is determined by the previous instruction. Address contents are the same as in Items (7) and (8).

(10) Write data to CG or DD RAM

	RS	R/W	DB_7							DB_0
Code	1	0	D	D	D	D	D	D	D	D

← Higher Order Bits   Lower Order Bits →

Writes binary 8 bit data DDDDDDDD to the CG or the DD RAM. Whether the CG or DD RAM is to be written into is determined by the previous specification of CG RAM or DD RAM address setting. After write, the address is automatically incremented or decremented by 1 according to entry mode. The entry mode also determines display shift.

(11) Read data from CG or DD RAM

	RS	R/W	DB_7							DB_0
Code	1	1	D	D	D	D	D	D	D	D

← Higher Order Bits   Lower Order Bits →

Reads binary 8 bit data DDDDDDDD from the CG or DD RAM. The previous designation determines whether the CG or DD RAM is to be read. Before entering the read instruction, you must execute either the CG RAM or DD RAM address set instruction. If you don't, the first read data will be invalidated. When serially executing the "read" instruction, the next address data is normally read from the second read. The "address set" instruction need not be executed just before the "read" instruction when shifting the cursor by cursor shift instruction (when reading out DD RAM). The cursor shift instruction operation is the same as that of the DD RAM's address set instruction.

After a read, the entry mode automatically increases or decreases the address by 1. However, display shift is not executed no matter what the entry mode is.

(Note) The address counter (AC) is automatically incremented or decremented by 1 after "write" instructions to either CG RAM or DD RAM. RAM data selected by the AC cannot than be read out even if "read" instructions are executed. The conditions for correct data read out are: execute either the address set instruction or cursor shift instruction (only with DD RAM), just before reading out execute the "read" instruction from the sebond time the "read" instruction is serial.

5.3 Instruction and display correspondence

(1) 8-bit operation, 8-digit x 1-line display (using internal reset)

Following table shows an example of 8-bit x 1-line display in 8-bit operation.

The HD44780 functions must be set by Function Set prior to display. Since the display data RAM can store data for 80 characters, as explained before, the RAM can be used for displays like the lightening board when combined with display shift operation.

Since the display shift operation changes display position only and DD RAM contents remain unchanged, display data entered first can be output when the return home operation is performed.

8 bit operation, 8-digit 1-line display example (using internal reset)

No.	Instruction	Display	Operation
1	Power supply ON (HD44780 is initialized by the internal reset circuit)	[ ]	Initialized. No display appears.
2	Function Set RS R/W DB_7 ——— DB_0 0 0 0 0 1 1 0 0 • •	[ ]	Sets to 8-bit operation and selects 1-line display lines and character font. (Number of display lines and character fonts cannot be changed hereafter.)
3	Display ON/OFF Control 0 0 0 0 0 0 1 1 1 0	[_]	Turns on display and cursor. Entire display is in space mode because of initialization.
4	Entry Mode Set 0 0 0 0 0 0 0 1 1 0	[_]	Sets mode to increment the address by one and to shift the cursor to the right at the time of write to the DD/CG RAM. Display is not shifted.
5	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 0 0 0	[H_]	Write "H". The DD RAM has already been selected by initialization when the power is turned on. The cursor is incremented by one and shifted to the right.
6	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 0 0 1	[HI_]	Writes "I".
7	⋮	⋮	
8	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 0 0 1	[HITACHI_]	Writes "I".
9	Entry Mode Set 0 0 0 0 0 0 0 1 1 1	[·HITACHI_]	Sets mode for display shift at the time of write.
10	Write Data to CG RAM/DD RAM 1 0 0 0 1 0 0 0 0 0	[ITACHI_]	Writes "Space".
11	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 1 0 1	[TACHI M_]	Writes "M".
12	⋮	⋮	
13	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 1 1 1	[MICROKO_]	Writes "O".
14	Cursor or Display Shift 0 0 0 0 0 1 0 0 • •	[MICROKO]	Shifts only the cursor position to the left.
15	Cursor or Display Shift 0 0 0 0 0 1 0 0 • •	[MICROKO]	Shifts only the cursor position to the left.
16	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 0 0 1 1	[ICROCO]	Writes "C" (correction). The display moves to the left.
17	Cursor or Diaplay Shift 0 0 0 0 0 1 1 1 • •	[MICROCO]	Shifts the display and cursor position to the right.
18	Cursor or Display Shift 0 0 0 0 0 1 0 1 • •	[MICROCO_]	Shifts display and cursor position to the right.
19	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 1 0 1	[ICROCOM_]	Writes "M".
20	⋮	⋮	
21	Return Home 0 0 0 0 0 0 0 0 1 0	[HITACHI]	Returns both display and cursor to the original position (Address 0).

(2) 4-bit operation, 8-digit x 1-line display (using internal reset)
The program must set functions prior to 4-bit operation. The following table shows an example. When power is turned on, 8-bit operation is automatically selected and the first write is performed as an 8-bit operation. Since nothing is connected to $DB_0 \sim DB_3$, a rewrite is then required. However, since one operation is completed in two access of 4-bit operation, a rewrite is needed as a function (see the following table).
Thus, $DB_4 \sim DB_7$ of the function set is written twice.

4 bit operation, 8-digit 1-line display (using internal reset)

No.	Instruction	Display	Operation
1	Power supply ON (HD44780 is initialized by the internal reset circuit)		Initialized. No display appears.
2	Function Set RS R/W DB_7 —— DB_4 0 0 0 0 1 0		Sets to 4-bit operation. In this case, operation is handled as 8 bits by initialization, and only this instruction completes with one write.
3	Function Set 0 0 0 0 1 0 0 0 0 0 • •		Sets 4-bit operation and selects 1-line display and 5 x 7 dot character font. 4-bit operation starts from this point on and resetting is needed. (Number of display lines and character fonts cannot be changed hereafter.)
4	Display ON/OFF Control 0 0 0 0 0 0 0 0 1 1 1 0	_	Turns on display and cursor. Entire display is in space mode because of initialization.
5	Entry Mode Set 0 0 0 0 0 0 0 0 0 1 1 0	_	Sets mode to increment the address by one and to shift the cursor to the right, at the time of write, to the DD/CG RAM. Display is not shifted.
6	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 0 1 0 0 0	H_	Writes "H". The cursor is incremented by one and shifts to the right.

Hereafter, control is the same as 8-bit operation.

(3) 8-bit operation, 8-digit x 2-line display
For 2-line display, the cursor automatically moves from the first to the second line after the 40th digit of the 1st line has been written. Thus, if there are only 8 characters in the first line, the DD RAM address must again be set after the 8th character is completed. (See the following table) Note that the first and second lines of the display shift are performed. In the example, the display shift is performed when the cursor is on the second line. However, if shift operation is performed when the cursor is on the first line, both the first and second lines move together. When you repeat the shift, the display of the second display will only move within each line many times.

8 bit operation, 8-digit x 2-line display example (using internal reset)

No.	Instruction	Display	Operation
1	Power supply ON (HD44780 is initialized by the internal reset circuit)	(blank)	Initialized. No display appears.
2	Function Set RS R/W DB_7 — DB_0 0 0 0 0 1 1 1 0 * *	(blank)	Sets to 8-bit operation and selects 2-line display and 5 x 7 dot character font.
3	Display ON/OFF Control 0 0 0 0 0 0 1 1 1 0	_	Turns on display and cursor. All display is in space mode because of initialization.
4	Entry Mode Set 0 0 0 0 0 0 0 1 1 0	_	Sets mode to increment the address by one and to shift the cursor to the right, at the time of write, to the DD/CG RAM. Display is not shifted.
5	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 0 0 0	H_	Write "H". The DD RAM has already been selected by initialization when the power is turned on. The cursor is incremented by one and shifted to the right.
6	⋮	⋮	
7	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 0 0 1	HITACHI_	Writes "I".
8	Set DD RAM Address 0 0 1 1 0 0 0 0 0 0	HITACHI _	Sets RAM address so that the cursor is positioned at the head of the 2nd line.
9	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 1 0 1	HITACHI M_	Writes "M".
10	⋮	⋮	
11	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 1 1 1	HITACHI MICROCO_	Writes "O".
12	Entry Mode Set 0 0 0 0 0 0 0 1 1 1	HITACHI MICROCO_	Sets mode for display shift at the time of write.
13	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 1 0 1	ITACHI ICROCOM_	Writes "M". Display is shifted to the right. The first and second lines' shift are operated at the same time.
14	⋮	⋮	
15	Return Home 0 0 0 0 0 0 0 0 1 0	HITACHI MICROCOM	Returns both display and cursor to the original position (Address 0).

6. Precaution on programming

(1) Instruction of function set
Perform the function at the head of program that accesses HD44780 before executing all instructions, and not change the data of the Instruction Register in the program. The data of function register can be changed by the program as follows;

a. • Changing of DL (Data Length)
- Perform the instruction appointed in 4.2 (2), when DL is changed from 8-bit length to 4-bit length mode.
- Perform the instruction appointed in 4.2 (1), when DL is changed from 4-bit length to 8-bit length mode.

b. • Changing of N (Column Number)
- Perform the instruction of function set after executing instruction of display clear or display off.

In this case, sequence of AC and DD RAM must be changed. Thus, rewrite the address set register after that.

c. • Changing of F (Font)
- There is no problem in this case, but for dual-line display, the font mode of 5 x 11 cannot be selected (this mode is forbidden by hardware).

When N or F is changed, power supply voltage for LCD must be changed. If not changed, crosstalk will appear, or contrast will be poor.

(2) Busy flag check
HD44780 is produced in the CMOS process, therefore internal executing time is long. Standard time is 40 μs ~ 1.6 ms. (This varies by instruction)
When the high speed MPU controls it, check the busy flag before performing instruction or reading data.
While internal operation is active, Enable signal is not accepted. (Enable signal at reading status register for checking busy flag is accepted) Busy flag signal is output through DB_7, as shown in Table 3, when RS = "0", R/W = "1", and Enable = "1".

(3) Input of unidentified instruction code
Undefined instruction code of HD44780 is only as follows;

RS	R/W	DB_7 ~ DB
0	0	0 ~

(Others are included to defined instruction)
When the undefined instruction code is loaded to HD44780, it accepts the code, but does not change the internal states (RAM and other status of Flags). Busy state, however continues for maximum 40 μs by the acceptance of the code.

Table 3 The relation between the operation and the combination of RS, R/W

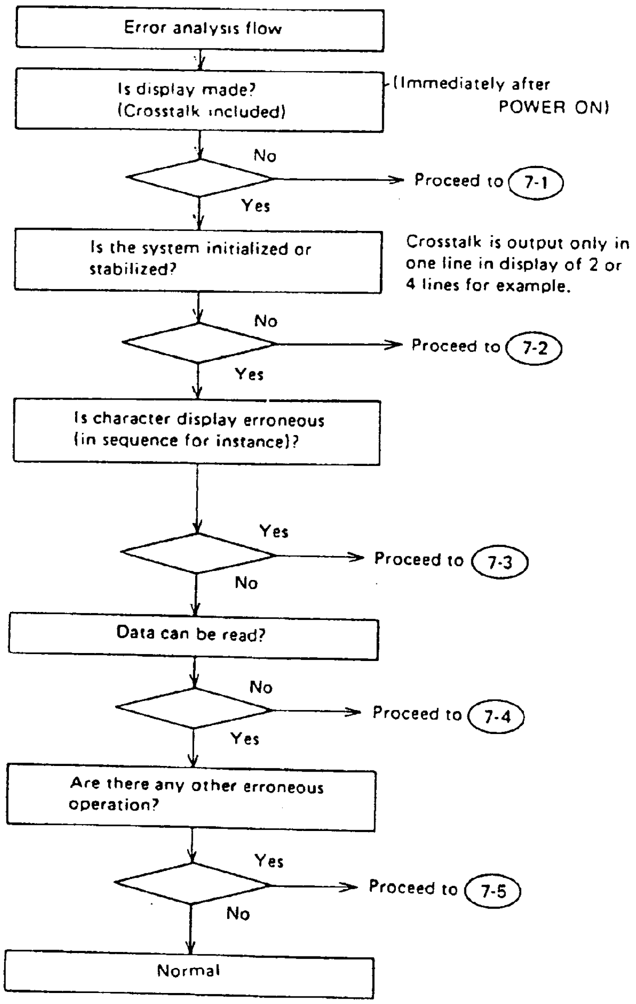
RS	RW	E	OPERATION
0	0		Write instruction code
0	1		Read busy flag and address counter
1	0		Write data
1	1		Read data

When performing data and instruction code by 4 bit, transfer RS, R/W every time.

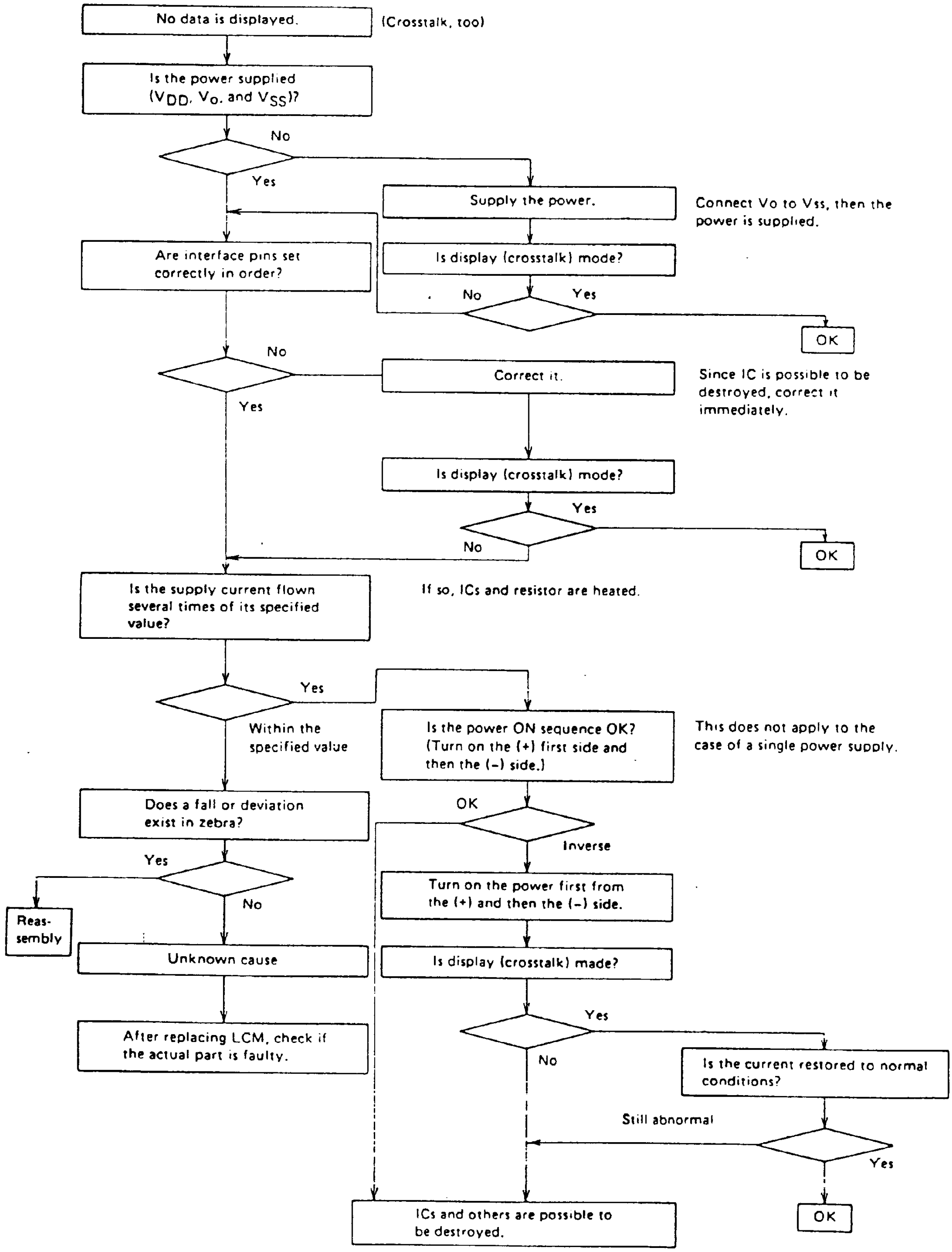
7. How to check trouble

· Follow the flowchart below to check errors.

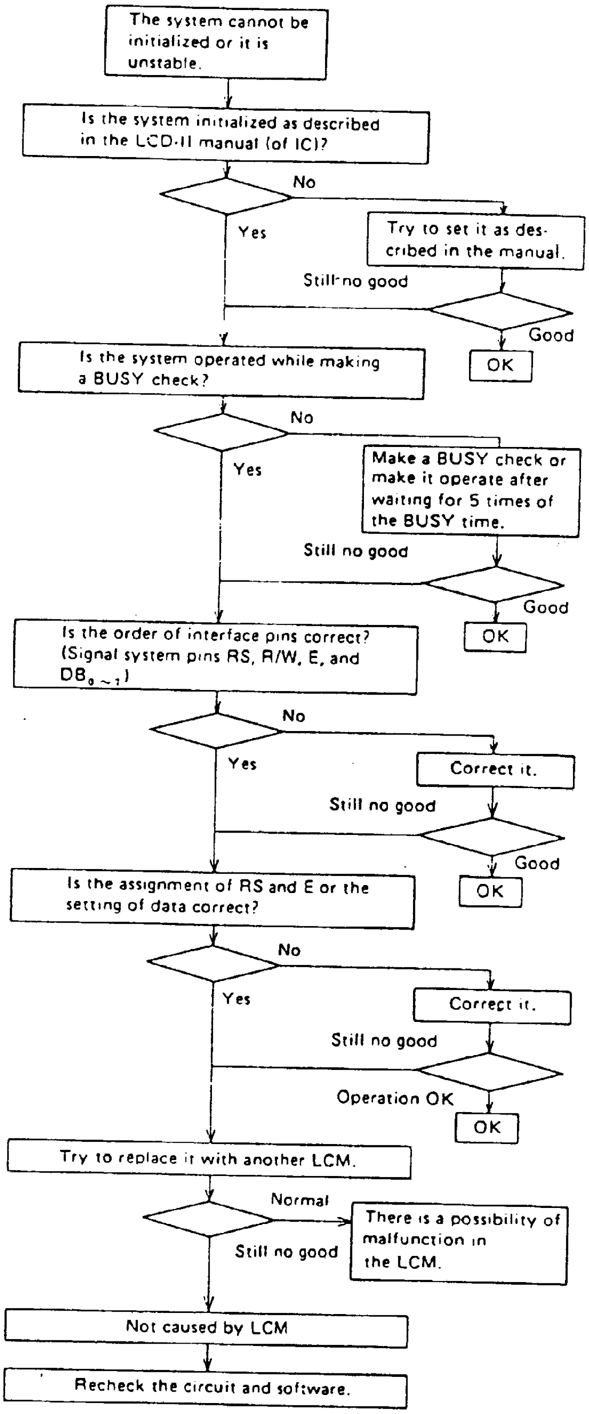
■ Error analysis flowchart



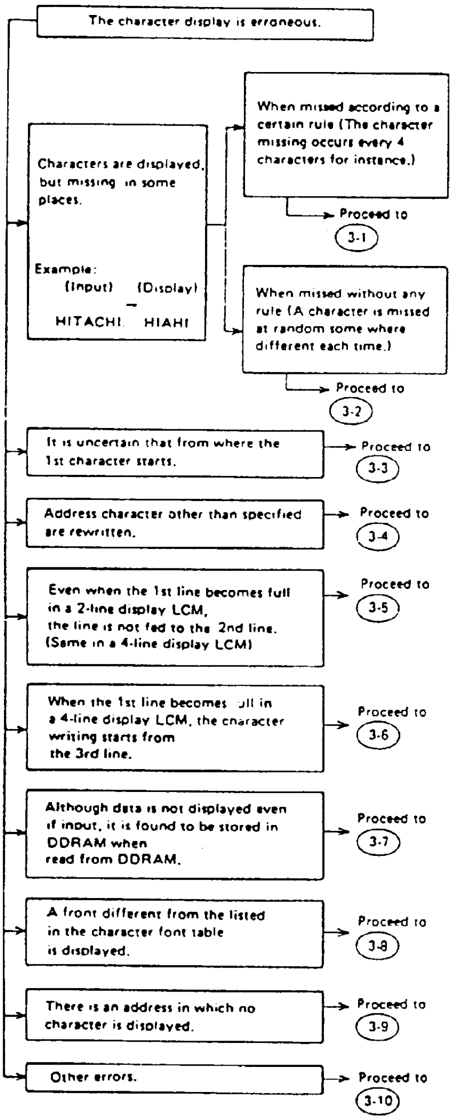
7.1 No data is displayed (Crosstalk too)



7.2 The system cannot be initialized or it is unstable.



7.3 The character display is erroneous.



(3-1)
Data is fed too fast. → Retry it while making a BUSY check. It is still too fast even when the BUSY check is made. → The function of LCD-II is no good.

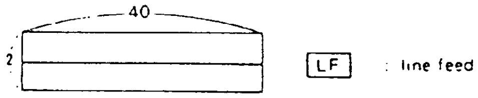
(3-2)
Data is fed too fast. → Retry it while making a BUSY check.

(3-3)
The address Set command is not included in the initialization.

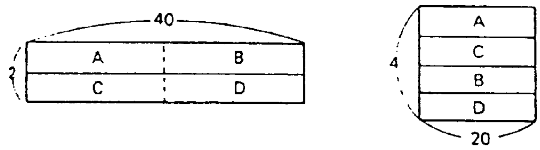
→ (Although the address is so designed to be set to "00" at the power ON according to the Power ON Reset function of the LCD-II itself, this Power ON Reset function does not work in some cases according to the power ON conditions.)

(3-4)
When no error exists in the software, the function of LCD-II is no good.

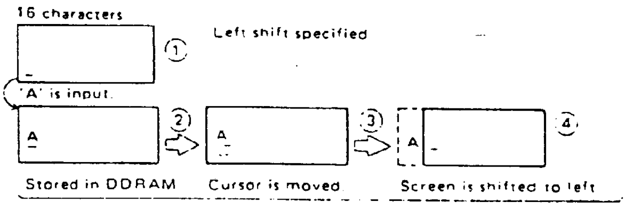
(3-5)
The 2-line display LCM is electrically composed of 40 characters x 2 lines, but it displays 16 characters or 20 characters partly. When 16 characters are written (in the 1st line) and the data at the 17th character is input as it is, it is entered in the 17th character in the 1st line and its is neither displayed on the screen. It is therefore necessary to set the address [LF] between the 16th caracter and 17th character.



(3-6)
The 4-line display LCM is composed as shown in the right figure. Consequently, when written continuously from the 1st line, the data is written as A → B. When displayed in 4 lines, the data is moved from the 1st line to the 3rd line. It is therefore necessary to set the address of [LF] in this case.



(3-7)
The display ON/OFF flag is turned to the OFF side. (This flag is by no means set unless turned to the ON side.).
When employing the shift function together, the screen is shifted each time a data is written and the data can not be seen on the screen in some cases. It is therefore necessary to correct the application of the shift function.



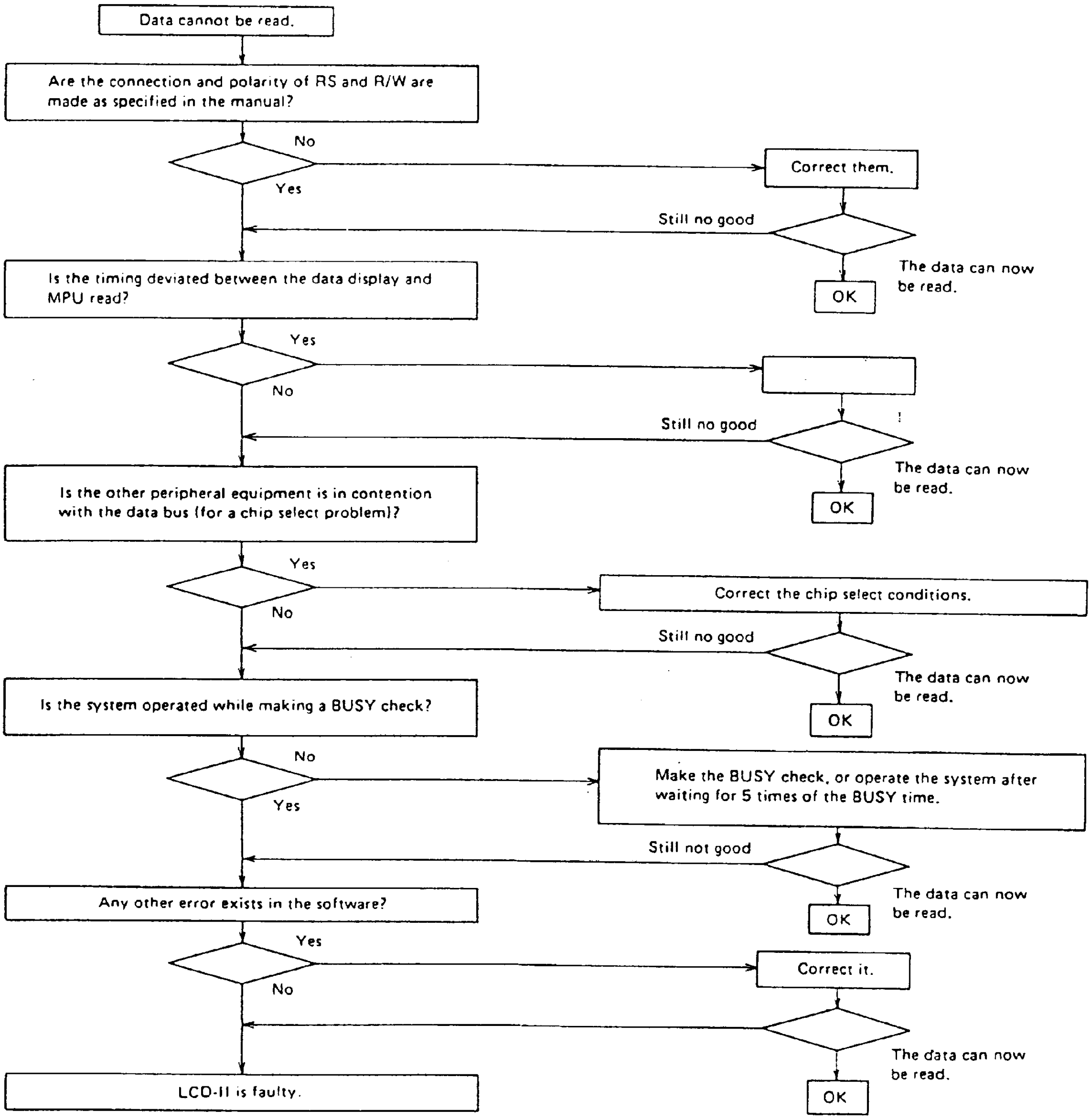
* Since this operation is carried out in a moment, what can be seen is the status of 1 and 4 only. Although not displayed in appearance, the data is stored in the DDRAM.

(3-8)
Defective CGROM font → IC is faulty.

(3-9)
If no error exists in the software, the IC is faulty.

(3-10)
Contact our agent for any other erroneous event.

7.4 Data cannot be read



7.5 Others

Others

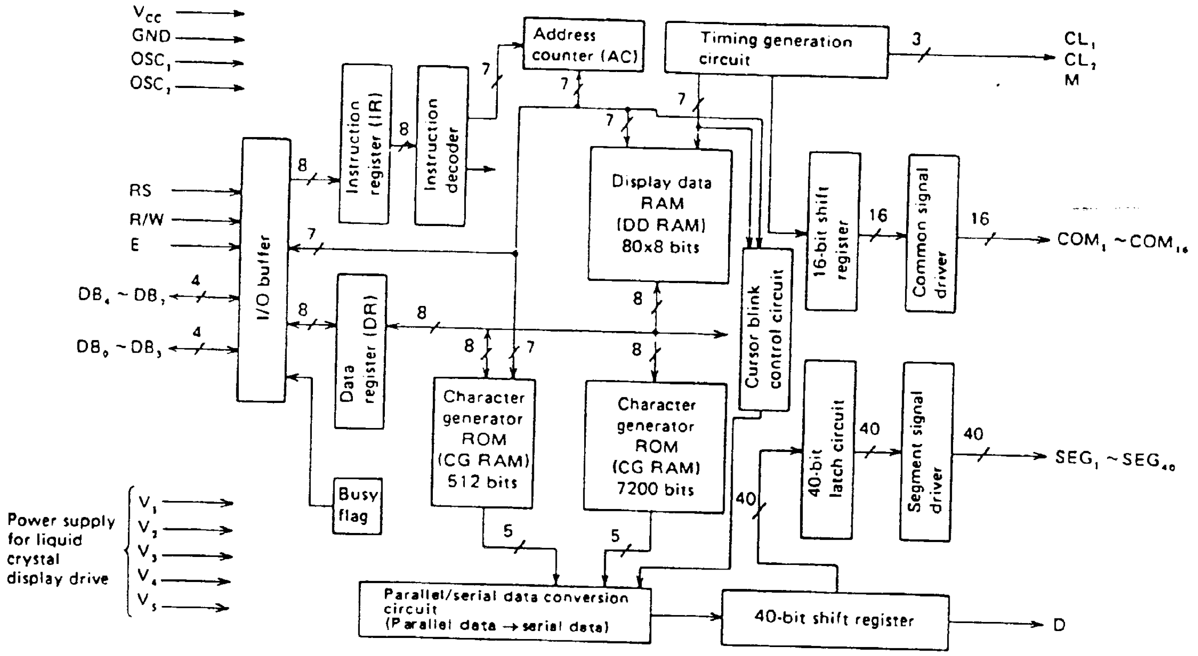
↓

Check the following:

- Use conditions
- Erroneous events
- Contents of operation before and after the error event occurrence
- Flowchart, if possible. (The program, if given, can not be decoded.)

8. Block diagram and function of each block

8.1 Block diagram of HD44780 interior



8.2 Function of each block

(1) Register

The HD44780 has two 8-bit registers, an instruction register (IR) and a data register (DR).

The IR stores instruction codes such as display clear and cursor shift, and address information for display data RAM (DD RAM) and character generator RAM (CG RAM). The IR can be written from the MPU but not read by the MPU.

The DR temporarily stores data to be written into the DD RAM or the CG RAM and data to be read out from DD RAM or CG RAM. Data written into the DR from the MPU is automatically written into the DD RAM or the CG RAM by internal operation. The DR is also used for data storage when reading data from the DD RAM or the CG RAM. When address information is written into the IR, data is read into the DR from the DD RAM or the CG RAM by internal operation. Data transfer to the MPU is then completed by the MPU reading DR. After the MPU reads the DR, data in the DD RAM or CG RAM at the next address is sent to the DR for the next read from the MPU. Register selector (RS) signals make their selection from these two registers.

HD44780U (LCD-II)

(Dot Matrix Liquid Crystal Display Controller/Driver)

HITACHI

Description

The HD44780U dot-matrix liquid crystal display controller and driver LSI displays alphanumerics, Japanese kana characters, and symbols. It can be configured to drive a dot-matrix liquid crystal display under the control of a 4- or 8-bit microprocessor. Since all the functions such as display RAM, character generator, and liquid crystal driver, required for driving a dot-matrix liquid crystal display are internally provided on one chip, a minimal system can be interfaced with this controller/driver.

A single HD44780U can display up to one 8-character line or two 8-character lines.

The HD44780U has pin function compatibility with the HD44780S which allows the user to easily replace an LCD-II with an HD44780U. The HD44780U character generator ROM is extended to generate 208 5 × 8 dot character fonts and 32 5 × 10 dot character fonts for a total of 240 different character fonts.

The low power supply (2.7V to 5.5V) of the HD44780U is suitable for any portable battery-driven product requiring low power dissipation.

Features

- 5 × 8 and 5 × 10 dot matrix possible
- Low power operation support:
  - 2.7 to 5.5V
- Wide range of liquid crystal display driver power
  - 3.0 to 11V
- Liquid crystal drive waveform
  - A (One line frequency AC waveform)
- Correspond to high speed MPU bus interface
  - 2 MHz (when V_{CC} = 5V)
- 4-bit or 8-bit MPU interface enabled
- 80 × 8-bit display RAM (80 characters max.)
- 9,920-bit character generator ROM for a total of 240 character fonts
  - 208 character fonts (5 × 8 dot)
  - 32 character fonts (5 × 10 dot)

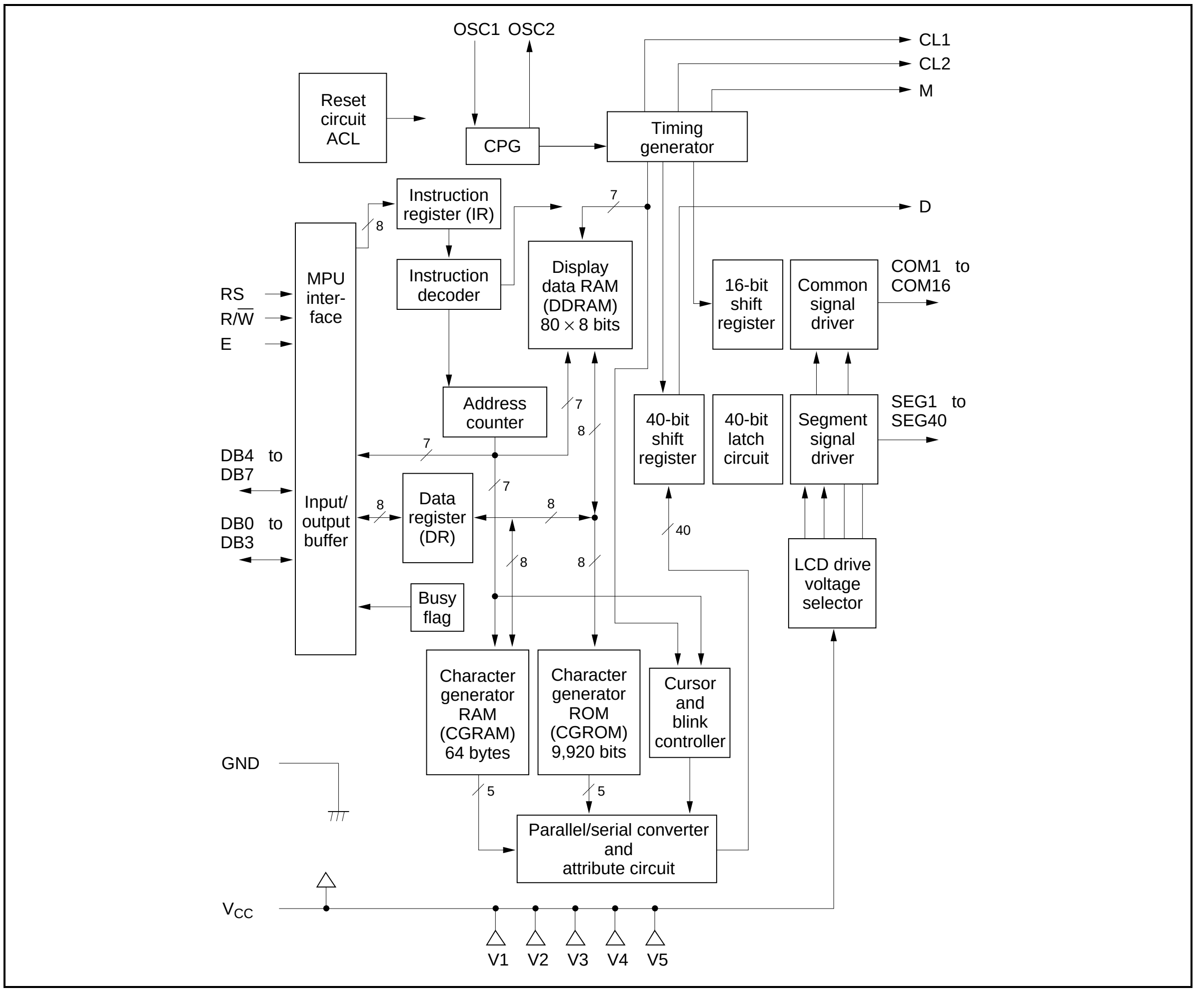
- 64×8-bit character generator RAM
  - — 8 character fonts (5×8 dot)
  - — 4 character fonts (5×10 dot)
- 16-common × 40-segment liquid crystal display driver
- Programmable duty cycles
  - — 1/8 for one line of 5×8 dots with cursor
  - — 1/11 for one line of 5×10 dots with cursor
  - — 1/16 for two lines of 5×8 dots with cursor
- Wide range of instruction functions:
  - — Display clear, cursor home, display on/off, cursor on/off, display character blink, cursor shift, display shift
- Pin function compatibility with HD44780S
- Automatic reset circuit that initializes the controller/driver after power on
- Internal oscillator with external resistors
- Low power consumption

Ordering Information

Type No.	Package	CGROM
HD44780UA00FS	FP-80B	Japanese standard font
HCD44780UA00	Chip	
HD44780UA00TF	TFP-80F	
HD44780UA02FS	FP-80B	European standard font
HCD44780UA02	Chip	
HD44780UA02TF	TFP-80F	
HD44780UBxxFS	FP-80B	Custom font
HCD44780UBxx	Chip	
HD44780UBxxTF	TFP-80F	

Note: xx: ROM code No.

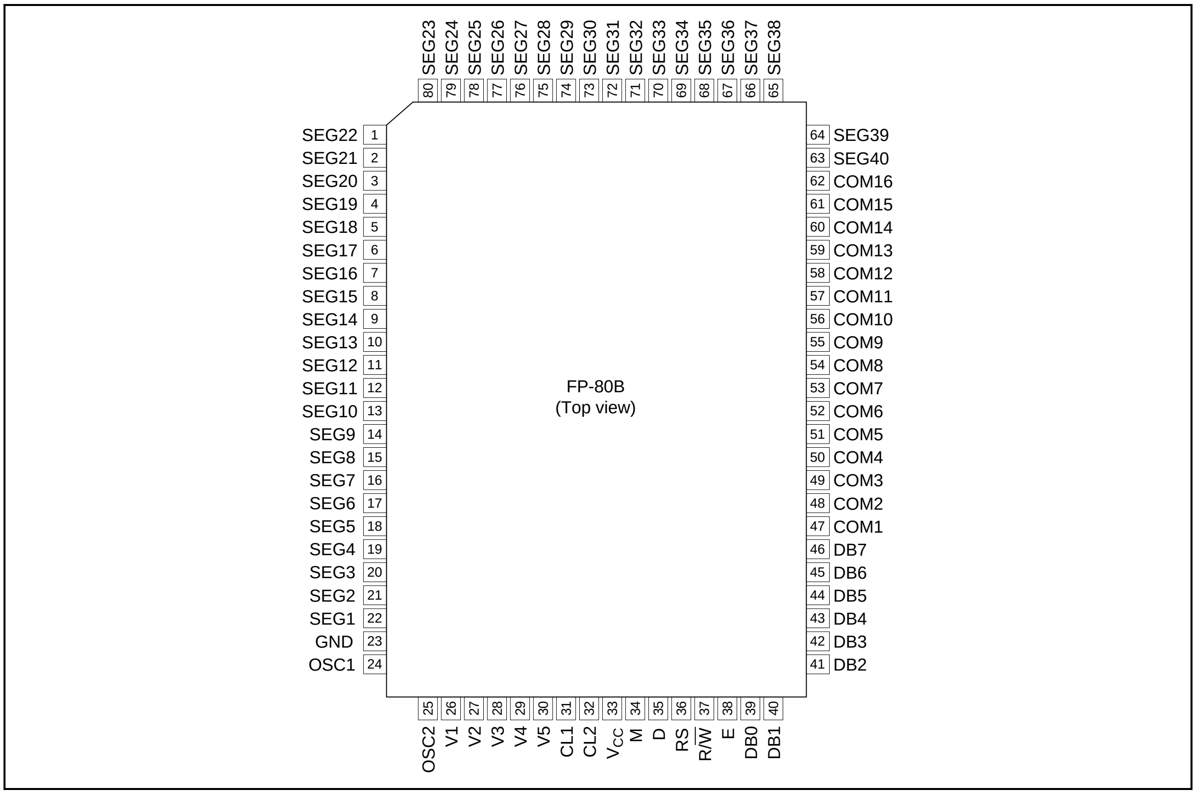
HD44780U Block Diagram



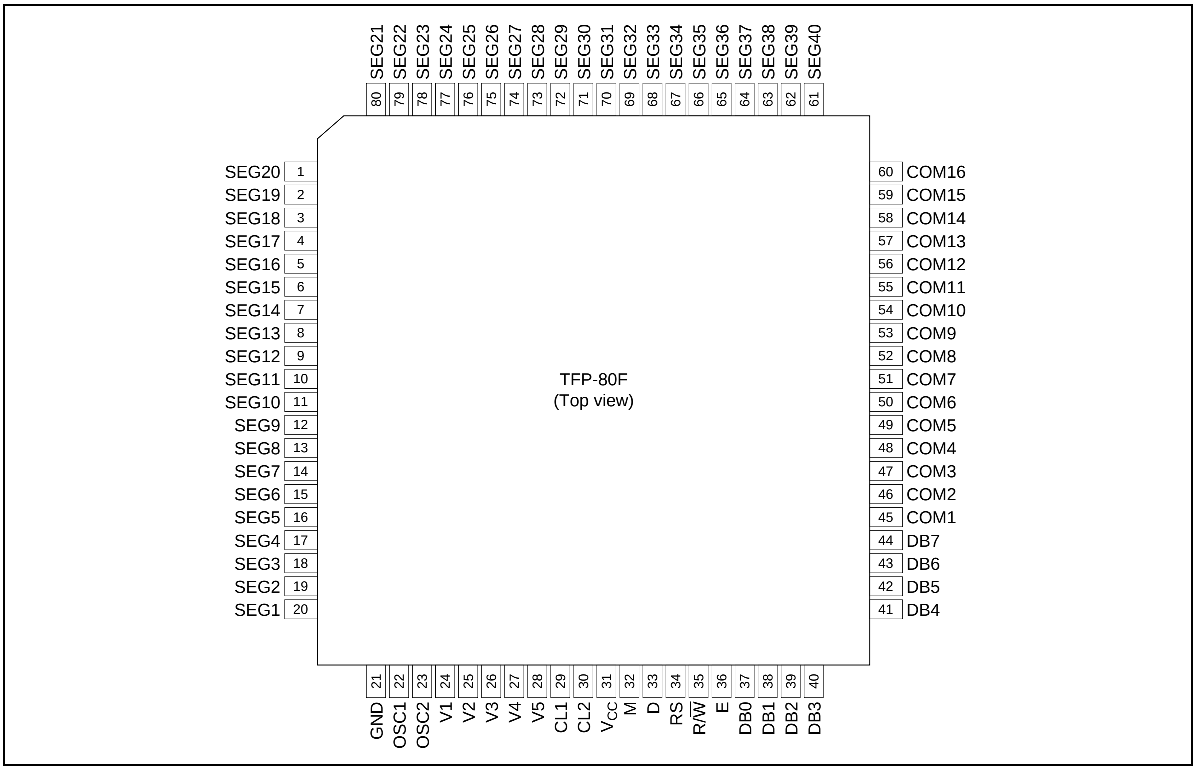
LCD-II Family Comparison

Item		HD44780S	HD44780U
Power supply voltage		5 V ±10%	2.7 to 5.5 V
Liquid crystal drive voltage VLCD	1/4 bias	3.0 to 11.0V	3.0 to 11.0V
	1/5 bias	4.6 to 11.0V	3.0 to 11.0V
Maximum display digits per chip		16 digits (8 digits × 2 lines)	16 digits (8 digits × 2 lines)
Display duty cycle		1/8, 1/11, and 1/16	1/8, 1/11, and 1/16
CGROM		7,200 bits (160 character fonts for 5 × 7 dot and 32 character fonts for 5 × 10 dot)	9,920 bits (208 character fonts for 5 × 8 dot and 32 character fonts for 5 × 10 dot)
CGRAM		64 bytes	64 bytes
DDRAM		80 bytes	80 bytes
Segment signals		40	40
Common signals		16	16
Liquid crystal drive waveform		A	A
Oscillator	Clock source	External resistor, external ceramic filter, or external clock	External resistor or external clock
	R_f oscillation frequency (frame frequency)	270 kHz ±30% (59 to 110 Hz for 1/8 and 1/16 duty cycles; 43 to 80 Hz for 1/11 duty cycle)	270 kHz ±30% (59 to 110 Hz for 1/8 and1/16 duty cycles; 43 to 80 Hz for 1/11 duty cycle)
	R_f resistance	91 kΩ ±2%	91 kΩ ±2% (when V_{cc} = 5V) 75 kΩ ±2% (when V_{cc} = 3V)
Instructions		Fully compatible within the HD44780S	
CPU bus timing		1 MHz	1 MHz (when V_{cc} = 3V) 2 MHz (when V_{cc} = 5V)
Package		FP-80 FP-80A	FP-80B TFP-80F

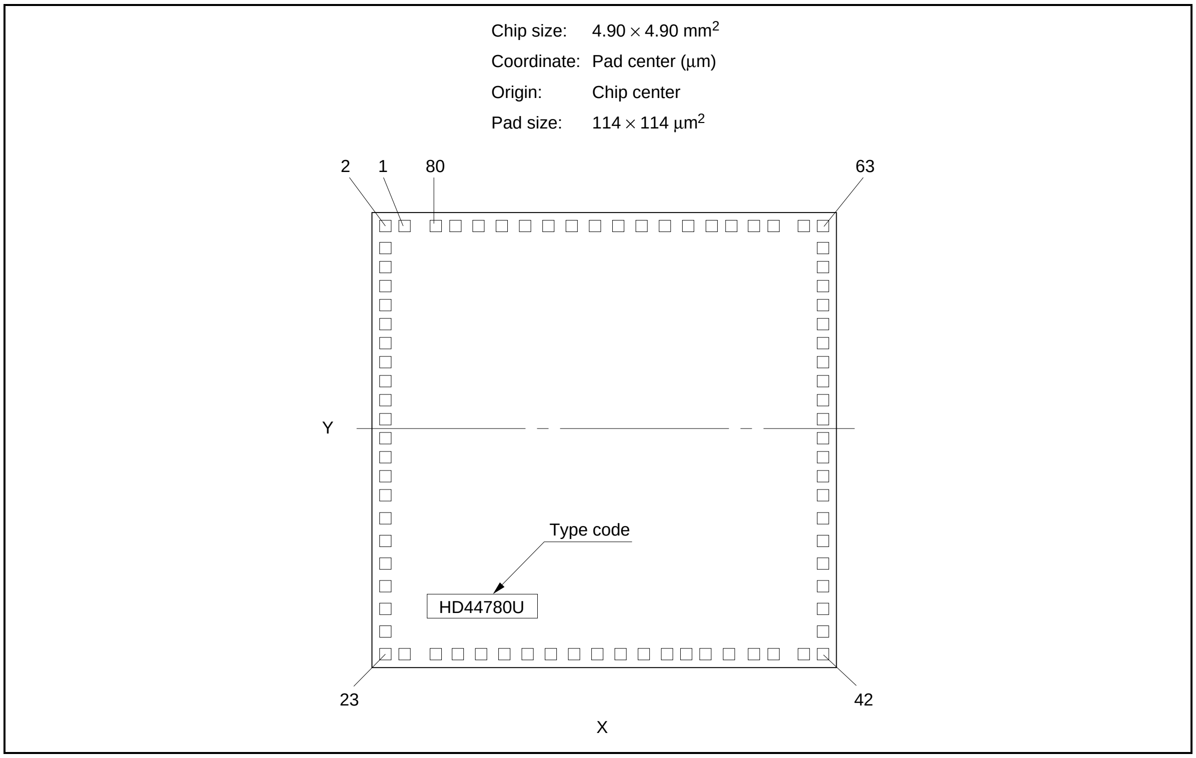
HD44780U Pin Arrangement (FP-80B)



HD44780U Pin Arrangement (TFP-80F)



HD44780U Pad Arrangement



HCD44780U Pad Location Coordinates

Pad No.	Function	Coordinate X (um)	Coordinate Y (um)	Pad No.	Function	Coordinate X (um)	Coordinate Y (um)
1	SEG22	–2100	2313	41	DB2	2070	–2290
2	SEG21	–2280	2313	42	DB3	2260	–2290
3	SEG20	–2313	2089	43	DB4	2290	–2099
4	SEG19	–2313	1833	44	DB5	2290	–1883
5	SEG18	–2313	1617	45	DB6	2290	–1667
6	SEG17	–2313	1401	46	DB7	2290	–1452
7	SEG16	–2313	1186	47	COM1	2313	–1186
8	SEG15	–2313	970	48	COM2	2313	–970
9	SEG14	–2313	755	49	COM3	2313	–755
10	SEG13	–2313	539	50	COM4	2313	–539
11	SEG12	–2313	323	51	COM5	2313	–323
12	SEG11	–2313	108	52	COM6	2313	–108
13	SEG10	–2313	–108	53	COM7	2313	108
14	SEG9	–2313	–323	54	COM8	2313	323
15	SEG8	–2313	–539	55	COM9	2313	539
16	SEG7	–2313	–755	56	COM10	2313	755
17	SEG6	–2313	–970	57	COM11	2313	970
18	SEG5	–2313	–1186	58	COM12	2313	1186
19	SEG4	–2313	–1401	59	COM13	2313	1401
20	SEG3	–2313	–1617	60	COM14	2313	1617
21	SEG2	–2313	–1833	61	COM15	2313	1833
22	SEG1	–2313	–2073	62	COM16	2313	2095
23	GND	–2280	–2290	63	SEG40	2296	2313
24	OSC1	–2080	–2290	64	SEG39	2100	2313
25	OSC2	–1749	–2290	65	SEG38	1617	2313
26	V1	–1550	–2290	66	SEG37	1401	2313
27	V2	–1268	–2290	67	SEG36	1186	2313
28	V3	–941	–2290	68	SEG35	970	2313
29	V4	–623	–2290	69	SEG34	755	2313
30	V5	–304	–2290	70	SEG33	539	2313
31	CL1	–48	–2290	71	SEG32	323	2313
32	CL2	142	–2290	72	SEG31	108	2313
33	V_{CC}	309	–2290	73	SEG30	–108	2313
34	M	475	–2290	74	SEG29	–323	2313
35	D	665	–2290	75	SEG28	–539	2313
36	RS	832	–2290	76	SEG27	–755	2313
37	$R/\overline{W}$	1022	–2290	77	SEG26	–970	2313
38	E	1204	–2290	78	SEG25	–1186	2313
39	DB0	1454	–2290	79	SEG24	–1401	2313
40	DB1	1684	–2290	80	SEG23	–1617	2313

Pin Functions

Signal	No. of Lines	I/O	Device Interfaced with	Function
RS	1	I	MPU	Selects registers. 0: Instruction register (for write) Busy flag: address counter (for read) 1: Data register (for write and read)
R/$\overline{W}$	1	I	MPU	Selects read or write. 0: Write 1: Read
E	1	I	MPU	Starts data read/write.
DB4 to DB7	4	I/O	MPU	Four high order bidirectional tristate data bus pins. Used for data transfer and receive between the MPU and the HD44780U. DB7 can be used as a busy flag.
DB0 to DB3	4	I/O	MPU	Four low order bidirectional tristate data bus pins. Used for data transfer and receive between the MPU and the HD44780U. These pins are not used during 4-bit operation.
CL1	1	O	Extension driver	Clock to latch serial data D sent to the extension driver
CL2	1	O	Extension driver	Clock to shift serial data D
M	1	O	Extension driver	Switch signal for converting the liquid crystal drive waveform to AC
D	1	O	Extension driver	Character pattern data corresponding to each segment signal
COM1 to COM16	16	O	LCD	Common signals that are not used are changed to non-selection waveforms. COM9 to COM16 are non-selection waveforms at 1/8 duty factor and COM12 to COM16 are non-selection waveforms at 1/11 duty factor.
SEG1 to SEG40	40	O	LCD	Segment signals
V1 to V5	5	—	Power supply	Power supply for LCD drive V_{CC} –V5 = 11 V (max)
V_{CC}, GND	2	—	Power supply	V_{CC}: 2.7V to 5.5V, GND: 0V
OSC1, OSC2	2	—	Oscillation resistor clock	When crystal oscillation is performed, a resistor must be connected externally. When the pin input is an external clock, it must be input to OSC1.

Function Description

Registers

The HD44780U has two 8-bit registers, an instruction register (IR) and a data register (DR).

The IR stores instruction codes, such as display clear and cursor shift, and address information for display data RAM (DDRAM) and character generator RAM (CGRAM). The IR can only be written from the MPU.

The DR temporarily stores data to be written into DDRAM or CGRAM and temporarily stores data to be read from DDRAM or CGRAM. Data written into the DR from the MPU is automatically written into DDRAM or CGRAM by an internal operation. The DR is also used for data storage when reading data from DDRAM or CGRAM. When address information is written into the IR, data is read and then stored into the DR from DDRAM or CGRAM by an internal operation. Data transfer between the MPU is then completed when the MPU reads the DR. After the read, data in DDRAM or CGRAM at the next address is sent to the DR for the next read from the MPU. By the register selector (RS) signal, these two registers can be selected (Table 1).

Busy Flag (BF)

When the busy flag is 1, the HD44780U is in the internal operation mode, and the next instruction will not be accepted. When RS = 0 and R/$\overline{W}$ = 1 (Table 1), the busy flag is output to DB7. The next instruction must be written after ensuring that the busy flag is 0.

Address Counter (AC)

The address counter (AC) assigns addresses to both DDRAM and CGRAM. When an address of an instruction is written into the IR, the address information is sent from the IR to the AC. Selection of either DDRAM or CGRAM is also determined concurrently by the instruction.

After writing into (reading from) DDRAM or CGRAM, the AC is automatically incremented by 1 (decremented by 1). The AC contents are then output to DB0 to DB6 when RS = 0 and R/$\overline{W}$ = 1 (Table 1).

Table 1 Register Selection

RS	R/$\overline{W}$	Operation
0	0	IR write as an internal operation (display clear, etc.)
0	1	Read busy flag (DB7) and address counter (DB0 to DB6)
1	0	DR write as an internal operation (DR to DDRAM or CGRAM)
1	1	DR read as an internal operation (DDRAM or CGRAM to DR)

Display Data RAM (DDRAM)

Display data RAM (DDRAM) stores display data represented in 8-bit character codes. Its extended capacity is 80 × 8 bits, or 80 characters. The area in display data RAM (DDRAM) that is not used for display can be used as general data RAM. See Figure 1 for the relationships between DDRAM addresses and positions on the liquid crystal display.

The DDRAM address (A_{DD}) is set in the address counter (AC) as hexadecimal.

- 1-line display (N = 0) (Figure 2)
  - — When there are fewer than 80 display characters, the display begins at the head position. For example, if using only the HD44780, 8 characters are displayed. See Figure 3.

    When the display shift operation is performed, the DDRAM address shifts. See Figure 3.

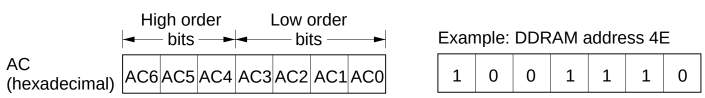


Figure 1 DDRAM Address

Display position (digit)	1	2	3	4	5		79	80
DDRAM address (hexadecimal)	00	01	02	03	04	....	4E	4F

Figure 2 1-Line Display

Display position	1	2	3	4	5	6	7	8
DDRAM address	00	01	02	03	04	05	06	07
For shift left	01	02	03	04	05	06	07	08
For shift right	4F	00	01	02	03	04	05	06

Figure 3 1-Line by 8-Character Display Example

- 2-line display (N = 1) (Figure 4)
  - — Case 1: When the number of display characters is less than 40 × 2 lines, the two lines are displayed from the head. Note that the first line end address and the second line start address are not consecutive. For example, when just the HD44780 is used, 8 characters × 2 lines are displayed. See Figure 5.

    When display shift operation is performed, the DDRAM address shifts. See Figure 5.

Display position	1	2	3	4	5		39	40
DDRAM address (hexadecimal)	00	01	02	03	04	....	26	27
	40	41	42	43	44	....	66	67

Figure 4 2-Line Display

Display position	1	2	3	4	5	6	7	8
DDRAM address	00	01	02	03	04	05	06	07
	40	41	42	43	44	45	46	47
For shift left	01	02	03	04	05	06	07	08
	41	42	43	44	45	46	47	48
For shift right	27	00	01	02	03	04	05	06
	67	40	41	42	43	44	45	46

Figure 5 2-Line by 8-Character Display Example

— Case 2: For a 16-character × 2-line display, the HD44780 can be extended using one 40-output extension driver. See Figure 6.

When display shift operation is performed, the DDRAM address shifts. See Figure 6.

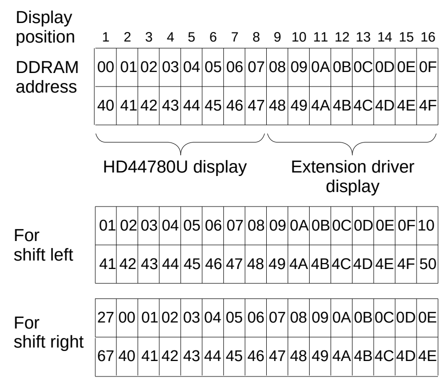


Figure 6 2-Line by 16-Character Display Example

Character Generator ROM (CGROM)

The character generator ROM generates 5 × 8 dot or 5 × 10 dot character patterns from 8-bit character codes (Table 4). It can generate 208 5 × 8 dot character patterns and 32 5 × 10 dot character patterns. User-defined character patterns are also available by mask-programmed ROM.

Character Generator RAM (CGRAM)

In the character generator RAM, the user can rewrite character patterns by program. For 5 × 8 dots, eight character patterns can be written, and for 5 × 10 dots, four character patterns can be written.

Write into DDRAM the character codes at the addresses shown as the left column of Table 4 to show the character patterns stored in CGRAM.

See Table 5 for the relationship between CGRAM addresses and data and display patterns.

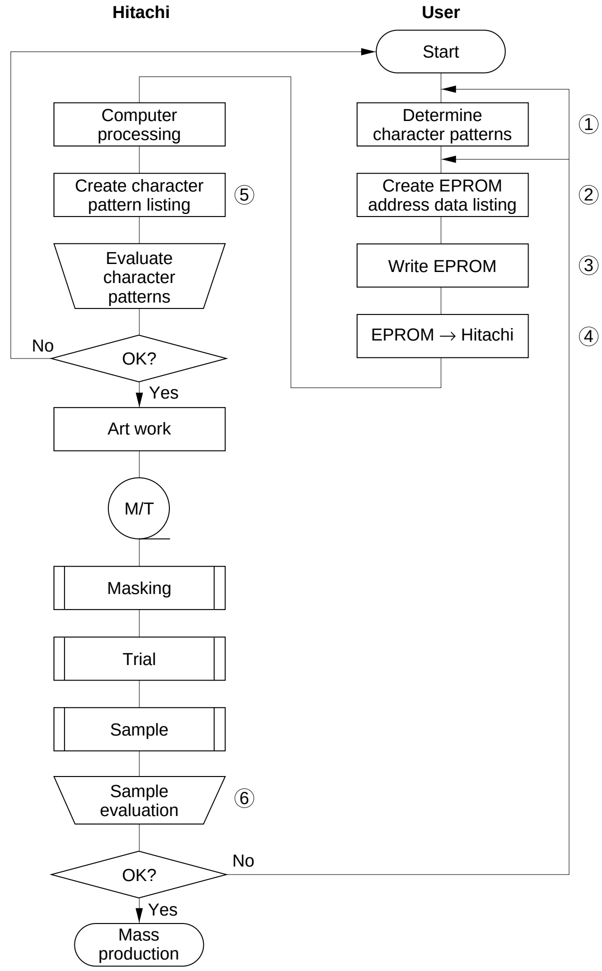
Areas that are not used for display can be used as general data RAM.

Modifying Character Patterns

- Character pattern development procedure

The following operations correspond to the numbers listed in Figure 7:

1. Determine the correspondence between character codes and character patterns.
2. Create a listing indicating the correspondence between EPROM addresses and data.
3. Program the character patterns into the EPROM.
4. Send the EPROM to Hitachi.
5. Computer processing on the EPROM is performed at Hitachi to create a character pattern listing, which is sent to the user.
6. If there are no problems within the character pattern listing, a trial LSI is created at Hitachi and samples are sent to the user for evaluation. When it is confirmed by the user that the character patterns are correctly written, mass production of the LSI proceeds at Hitachi.



Note: For a description of the numbers used in this figure, refer to the preceding page.

Figure 7 Character Pattern Development Procedure

- Programming character patterns

  This section explains the correspondence between addresses and data used to program character patterns in EPROM. The HD44780U character generator ROM can generate 208 5 × 8 dot character patterns and 32 5 × 10 dot character patterns for a total of 240 different character patterns.

  — Character patterns

  EPROM address data and character pattern data correspond with each other to form a 5 × 8 or 5 × 10 dot character pattern (Tables 2 and 3).

Table 2 Example of Correspondence between EPROM Address Data and Character Pattern (5 × 8 Dots)

EPROM Address												Data					
A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	O4	O3	O2	O1	O0 (LSB)	
								0	0	0	0	1	0	0	0	0	
								0	0	0	1	1	0	0	0	0	
								0	0	1	0	1	0	1	1	0	
								0	0	1	1	1	1	0	0	1	
								0	1	0	0	1	0	0	0	1	
								0	1	0	1	1	0	0	0	1	
								0	1	1	0	1	1	1	1	0	
0	1	1	0	0	0	1	0	0	1	1	1	0	0	0	0	0	← Cursor position
								1	0	0	0	0	0	0	0	0	
								1	0	0	1	0	0	0	0	0	
								1	0	1	0	0	0	0	0	0	
								1	0	1	1	0	0	0	0	0	
								1	1	0	0	0	0	0	0	0	
								1	1	0	1	0	0	0	0	0	
								1	1	1	0	0	0	0	0	0	
								1	1	1	1	0	0	0	0	0	
Character code								Line position									

Notes: 1. EPROM addresses A11 to A4 correspond to a character code.
2. EPROM addresses A3 to A0 specify a line position of the character pattern.
3. EPROM data O4 to O0 correspond to character pattern data.
4. EPROM data O5 to O7 must be specified as 0.
5. A lit display position (black) corresponds to a 1.
6. Line 9 and the following lines must be blanked with 0s for a 5 × 8 dot character fonts.

— Handling unused character patterns

1. EPROM data outside the character pattern area: Always input 0s.
2. EPROM data in CGRAM area: Always input 0s. (Input 0s to EPROM addresses 00H to FFH.)
3. EPROM data used when the user does not use any HD44780U character pattern: According to the user application, handled in one of the two ways listed as follows.

a. When unused character patterns are not programmed: If an unused character code is written into DDRAM, all its dots are lit. By not programing a character pattern, all of its bits become lit. (This is due to the EPROM being filled with 1s after it is erased.)

b. When unused character patterns are programmed as 0s: Nothing is displayed even if unused character codes are written into DDRAM. (This is equivalent to a space.)

Table 3 Example of Correspondence between EPROM Address Data and Character Pattern (5 × 10 Dots)

EPROM Address												Data					
A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	O4	O3	O2	O1	O0 (LSB)	
								0	0	0	0	0	0	0	0	0	
								0	0	0	1	0	0	0	0	0	
								0	0	1	0	0	1	1	0	1	
								0	0	1	1	1	0	0	1	1	
								0	1	0	0	1	0	0	0	1	
								0	1	0	1	1	0	0	0	1	
								0	1	1	0	0	1	1	1	1	
0	1	0	1	0	0	1	0	0	1	1	1	0	0	0	0	1	
								1	0	0	0	0	0	0	0	1	
								1	0	0	1	0	0	0	0	1	
								1	0	1	0	0	0	0	0	0	← Cursor position
								1	0	1	1	0	0	0	0	0	
								1	1	0	0	0	0	0	0	0	
								1	1	0	1	0	0	0	0	0	
								1	1	1	0	0	0	0	0	0	
								1	1	1	1	0	0	0	0	0	

Character code (A11–A4); Line position (A3–A0)

Notes: 1. EPROM addresses A11 to A3 correspond to a character code.
2. EPROM addresses A3 to A0 specify a line position of the character pattern.
3. EPROM data O4 to O0 correspond to character pattern data.
4. EPROM data O5 to O7 must be specified as 0.
5. A lit display position (black) corresponds to a 1.
6. Line 11 and the following lines must be blanked with 0s for a 5 × 10 dot character fonts.

Table 4 Correspondence between Character Codes and Character Patterns (ROM Code: A00)

Lower 4 Bits \ Upper 4 Bits	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
xxxx0000	CG RAM (1)			0	@	P	`	p				ー	タ	ミ	α	p
xxxx0001	(2)		!	1	A	Q	a	q			。	ア	チ	ム	ä	q
xxxx0010	(3)		"	2	B	R	b	r			「	イ	ツ	メ	β	θ
xxxx0011	(4)		#	3	C	S	c	s			」	ウ	テ	モ	ε	∞
xxxx0100	(5)		$	4	D	T	d	t			、	エ	ト	ヤ	μ	Ω
xxxx0101	(6)		%	5	E	U	e	u			・	オ	ナ	ユ	σ	ü
xxxx0110	(7)		&	6	F	V	f	v			ヲ	カ	ニ	ヨ	ρ	Σ
xxxx0111	(8)		'	7	G	W	g	w			ァ	キ	ヌ	ラ	g	π
xxxx1000	(1)		(	8	H	X	h	x			ィ	ク	ネ	リ	√	x̄
xxxx1001	(2)		)	9	I	Y	i	y			ゥ	ケ	ノ	ル	⁻¹	y
xxxx1010	(3)		*	:	J	Z	j	z			ェ	コ	ハ	レ	j	千
xxxx1011	(4)		+	;	K	[	k	{			ォ	サ	ヒ	ロ	ˣ	万
xxxx1100	(5)		,	<	L	¥	l	|			ャ	シ	フ	ワ	¢	円
xxxx1101	(6)		-	=	M	]	m	}			ュ	ス	ヘ	ン	£	÷
xxxx1110	(7)		.	>	N	^	n	→			ョ	セ	ホ	゛	ñ	
xxxx1111	(8)		/	?	O	_	o	←			ッ	ソ	マ	゜	ö	█

Note: The user can specify any pattern for character-generator RAM.

Table 4 Correspondence between Character Codes and Character Patterns (ROM Code: A02)



Table 5 Relationship between CGRAM Addresses, Character Codes (DDRAM) and Character Patterns (CGRAM Data)

For 5 × 8 dot character patterns

Character Codes (DDRAM data) 7 6 5 4 3 2 1 0 (High … Low)	CGRAM Address 5 4 3 (High)	CGRAM Address 2 1 0 (Low)	Character Patterns (CGRAM data) 7 6 5 (High)	Character Patterns (CGRAM data) 4 3 2 1 0 (Low)	
0 0 0 0 * 0 0 0	0 0 0	0 0 0	* * *	1 1 1 1 0	Character pattern (1)
		0 0 1		1 0 0 0 1	
		0 1 0		1 0 0 0 1	
		0 1 1		1 1 1 1 0	
		1 0 0		1 0 1 0 0	
		1 0 1		1 0 0 1 0	
		1 1 0		1 0 0 0 1	
		1 1 1	* * *	0 0 0 0 0	Cursor position
0 0 0 0 * 0 0 1	0 0 1	0 0 0	* * *	1 0 0 0 1	Character pattern (2)
		0 0 1		0 1 0 1 0	
		0 1 0		1 1 1 1 1	
		0 1 1		0 0 1 0 0	
		1 0 0		1 1 1 1 1	
		1 0 1		0 0 1 0 0	
		1 1 0		0 0 1 0 0	
		1 1 1	* * *	0 0 0 0 0	Cursor position
		0 0 0	* * *		
		0 0 1			
0 0 0 0 * 1 1 1	1 1 1				
		1 0 0			
		1 0 1			
		1 1 0			
		1 1 1	* * *		

Notes: 1. Character code bits 0 to 2 correspond to CGRAM address bits 3 to 5 (3 bits: 8 types).

2. CGRAM address bits 0 to 2 designate the character pattern line position. The 8th line is the cursor position and its display is formed by a logical OR with the cursor.

   Maintain the 8th line data, corresponding to the cursor display position, at 0 as the cursor display.

   If the 8th line data is 1, 1 bits will light up the 8th line regardless of the cursor presence.

3. Character pattern row positions correspond to CGRAM data bits 0 to 4 (bit 4 being at the left).

4. As shown Table 5, CGRAM character patterns are selected when character code bits 4 to 7 are all 0. However, since character code bit 3 has no effect, the R display example above can be selected by either character code 00H or 08H.

5. 1 for CGRAM data corresponds to display selection and 0 to non-selection.

* Indicates no effect.

Table 5 Relationship between CGRAM Addresses, Character Codes (DDRAM) and Character Patterns (CGRAM Data) (cont)

For 5 × 10 dot character patterns

Character Codes (DDRAM data)	CGRAM Address		Character Patterns (CGRAM data)		
7 6 5 4 3 2 1 0	5 4	3 2 1 0	7 6 5	4 3 2 1 0	
High Low	High	Low	High	Low	
		0 0 0 0	* * *	0 0 0 0 0	Character pattern
		0 0 0 1		0 0 0 0 0	
		0 0 1 0		1 0 1 1 0	
		0 0 1 1		1 1 0 0 1	
		0 1 0 0		1 0 0 0 1	
0 0 0 0 * 0 0 *	0 0	0 1 0 1		1 0 0 0 1	
		0 1 1 0		1 1 1 1 0	
		0 1 1 1		1 0 0 0 0	
		1 0 0 0		1 0 0 0 0	
		1 0 0 1		1 0 0 0 0	
		1 0 1 0	* * *	0 0 0 0 0	Cursor position
		1 0 1 1	* * *	* * * * *	
		1 1 0 0			
		1 1 0 1			
		1 1 1 0			
		1 1 1 1	* * *	* * * * *	
		0 0 0 0	* * *		
		0 0 0 1			
0 0 0 0 * 1 1 *	1 1	1 0 0 1			
		1 0 1 0	* * *		
		1 0 1 1	* * *	* * * * *	
		1 1 0 0			
		1 1 0 1			
		1 1 1 0			
		1 1 1 1	* * *	* * * * *	

Notes: 1. Character code bits 1 and 2 correspond to CGRAM address bits 4 and 5 (2 bits: 4 types).

2. CGRAM address bits 0 to 3 designate the character pattern line position. The 11th line is the cursor position and its display is formed by a logical OR with the cursor.
Maintain the 11th line data corresponding to the cursor display positon at 0 as the cursor display.
If the 11th line data is "1", "1" bits will light up the 11th line regardless of the cursor presence.
Since lines 12 to 16 are not used for display, they can be used for general data RAM.

3. Character pattern row positions are the same as 5 × 8 dot character pattern positions.

4. CGRAM character patterns are selected when character code bits 4 to 7 are all 0.
However, since character code bits 0 and 3 have no effect, the P display example above can be selected by character codes 00H, 01H, 08H, and 09H.

5. 1 for CGRAM data corresponds to display selection and 0 to non-selection.

* Indicates no effect.

Timing Generation Circuit

The timing generation circuit generates timing signals for the operation of internal circuits such as DDRAM, CGROM and CGRAM. RAM read timing for display and internal operation timing by MPU access are generated separately to avoid interfering with each other. Therefore, when writing data to DDRAM, for example, there will be no undesirable interferences, such as flickering, in areas other than the display area.

Liquid Crystal Display Driver Circuit

The liquid crystal display driver circuit consists of 16 common signal drivers and 40 segment signal drivers. When the character font and number of lines are selected by a program, the required common signal drivers automatically output drive waveforms, while the other common signal drivers continue to output non-selection waveforms.

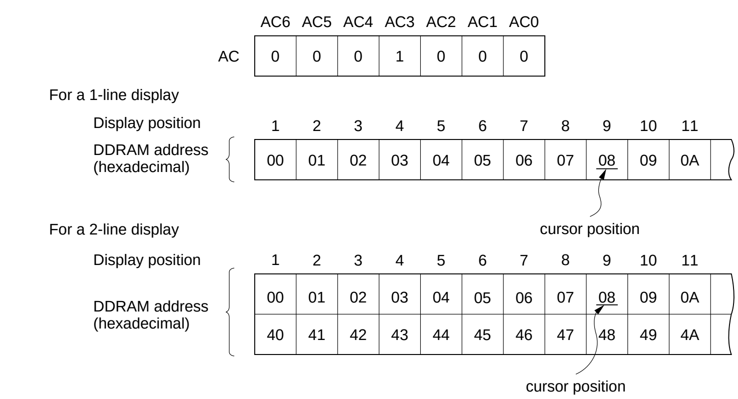
Sending serial data always starts at the display data character pattern corresponding to the last address of the display data RAM (DDRAM).

Since serial data is latched when the display data character pattern corresponding to the starting address enters the internal shift register, the HD44780U drives from the head display.

Cursor/Blink Control Circuit

The cursor/blink control circuit generates the cursor or character blinking. The cursor or the blinking will appear with the digit located at the display data RAM (DDRAM) address set in the address counter (AC).

For example (Figure 8), when the address counter is 08H, the cursor position is displayed at DDRAM address 08H.



Note: The cursor or blinking appears when the address counter (AC) selects the character generator RAM (CGRAM). However, the cursor and blinking become meaningless. The cursor or blinking is displayed in the meaningless position when the AC is a CGRAM address.

Figure 8 Cursor/Blink Display Example

Interfacing to the MPU

The HD44780U can send data in either two 4-bit operations or one 8-bit operation, thus allowing interfacing with 4- or 8-bit MPUs.

- For 4-bit interface data, only four bus lines (DB4 to DB7) are used for transfer. Bus lines DB0 to DB3 are disabled. The data transfer between the HD44780U and the MPU is completed after the 4-bit data has been transferred twice. As for the order of data transfer, the four high order bits (for 8-bit operation, DB4 to DB7) are transferred before the four low order bits (for 8-bit operation, DB0 to DB3).

  The busy flag must be checked (one instruction) after the 4-bit data has been transferred twice. Two more 4-bit operations then transfer the busy flag and address counter data.
- For 8-bit interface data, all eight bus lines (DB0 to DB7) are used.

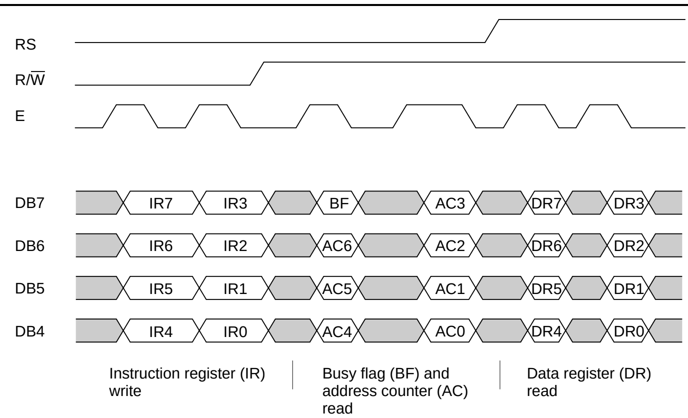


Figure 9 4-Bit Transfer Example

Reset Function

Initializing by Internal Reset Circuit

An internal reset circuit automatically initializes the HD44780U when the power is turned on. The following instructions are executed during the initialization. The busy flag (BF) is kept in the busy state until the initialization ends (BF = 1). The busy state lasts for 10 ms after V_{CC} rises to 4.5 V.

1. Display clear
2. Function set:
   DL = 1; 8-bit interface data
   N = 0; 1-line display
   F = 0; 5 × 8 dot character font
3. Display on/off control:
   D = 0; Display off
   C = 0; Cursor off
   B = 0; Blinking off
4. Entry mode set:
   I/D = 1; Increment by 1
   S = 0; No shift

Note: If the electrical characteristics conditions listed under the table Power Supply Conditions Using Internal Reset Circuit are not met, the internal reset circuit will not operate normally and will fail to initialize the HD44780U. For such a case, initial-ization must be performed by the MPU as explained in the section, Initializing by Instruction.

Instructions

Outline

Only the instruction register (IR) and the data register (DR) of the HD44780U can be controlled by the MPU. Before starting the internal operation of the HD44780U, control information is temporarily stored into these registers to allow interfacing with various MPUs, which operate at different speeds, or various peripheral control devices. The internal operation of the HD44780U is determined by signals sent from the MPU. These signals, which include register selection signal (RS), read/

write signal (R/$\overline{W}$), and the data bus (DB0 to DB7), make up the HD44780U instructions (Table 6). There are four categories of instructions that:

- Designate HD44780U functions, such as display format, data length, etc.
- Set internal RAM addresses
- Perform data transfer with internal RAM
- Perform miscellaneous functions

Normally, instructions that perform data transfer with internal RAM are used the most. However, auto-incrementation by 1 (or auto-decrementation by 1) of internal HD44780U RAM addresses after each data write can lighten the program load of the MPU. Since the display shift instruction (Table 11) can perform concurrently with display data write, the user can minimize system development time with maximum programming efficiency.

When an instruction is being executed for internal operation, no instruction other than the busy flag/address read instruction can be executed.

Because the busy flag is set to 1 while an instruction is being executed, check it to make sure it is 0 before sending another instruction from the MPU.

Note: Be sure the HD44780U is not in the busy state (BF = 0) before sending an instruction from the MPU to the HD44780U. If an instruction is sent without checking the busy flag, the time between the first instruction and next instruction will take much longer than the instruction time itself. Refer to Table 6 for the list of each instruc-tion execution time.

Table 6 Instructions

	Code											Execution Time (max) (when f_{cp} or
Instruction	**RS**	**R/$\overline{W}$**	**DB7**	**DB6**	**DB5**	**DB4**	**DB3**	**DB2**	**DB1**	**DB0**	**Description**	**f_{osc} is 270 kHz)**
Clear display	0	0	0	0	0	0	0	0	0	1	Clears entire display and sets DDRAM address 0 in address counter.	
Return home	0	0	0	0	0	0	0	0	1	—	Sets DDRAM address 0 in address counter. Also returns display from being shifted to original position. DDRAM contents remain unchanged.	1.52 ms
Entry mode set	0	0	0	0	0	0	0	1	I/D	S	Sets cursor move direction and specifies display shift. These operations are performed during data write and read.	37 µs
Display on/off control	0	0	0	0	0	0	1	D	C	B	Sets entire display (D) on/off, cursor on/off (C), and blinking of cursor position character (B).	37 µs
Cursor or display shift	0	0	0	0	0	1	S/C	R/L	—	—	Moves cursor and shifts display without changing DDRAM contents.	37 µs
Function set	0	0	0	0	1	DL	N	F	—	—	Sets interface data length (DL), number of display lines (N), and character font (F).	37 µs
Set CGRAM address	0	0	0	1	ACG	ACG	ACG	ACG	ACG	ACG	Sets CGRAM address. CGRAM data is sent and received after this setting.	37 µs
Set DDRAM address	0	0	1	ADD	ADD	ADD	ADD	ADD	ADD	ADD	Sets DDRAM address. DDRAM data is sent and received after this setting.	37 µs
Read busy flag & address	0	1	BF	AC	AC	AC	AC	AC	AC	AC	Reads busy flag (BF) indicating internal operation is being performed and reads address counter contents.	0 µs

Table 6 Instructions (cont)

Instruction	RS	R/$\overline{W}$	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0	Description	Execution Time (max) (when f_{cp} or f_{OSC} is 270 kHz)
Write data to CG or DDRAM	1	0	Write data	Writes data into DDRAM or CGRAM.	37 µs t_{ADD} = 4 µs*
Read data from CG or DDRAM	1	1	Read data	Reads data from DDRAM or CGRAM.	37 µs t_{ADD} = 4 µs*
	I/D I/D S S/C S/C R/L R/L DL N F BF BF	= 1: = 0: = 1: = 1: = 0: = 1: = 0: = 1: = 1: = 1: = 1: = 0:	Increment Decrement Accompanies display shift Display shift Cursor move Shift to the right Shift to the left 8 bits, DL = 0: 4 bits 2 lines, N = 0: 1 line 5 × 10 dots, F = 0: 5 × 8 dots Internally operating Instructions acceptable	DDRAM: Display data RAM CGRAM: Character generator RAM ACG: CGRAM address ADD: DDRAM address (corresponds to cursor address) AC: Address counter used for both DD and CGRAM addresses	Execution time changes when frequency changes Example: When f_{cp} or f_{OSC} is 250 kHz, $37\ \mu s \times \frac{270}{250} = 40\ \mu s$

Note: — indicates no effect.

* After execution of the CGRAM/DDRAM data write or read instruction, the RAM address counter is incremented or decremented by 1. The RAM address counter is updated after the busy flag turns off. In Figure 10, t_{ADD} is the time elapsed after the busy flag turns off until the address counter is updated.

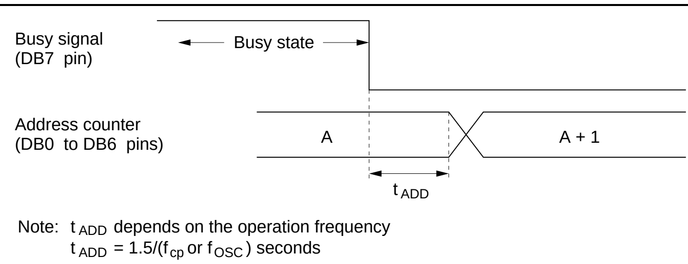


Figure 10 Address Counter Update

Instruction Description

Clear Display

Clear display writes space code 20H (character pattern for character code 20H must be a blank pattern) into all DDRAM addresses. It then sets DDRAM address 0 into the address counter, and returns the display to its original status if it was shifted. In other words, the display disappears and the cursor or blinking goes to the left edge of the display (in the first line if 2 lines are displayed). It also sets I/D to 1 (increment mode) in entry mode. S of entry mode does not change.

Return Home

Return home sets DDRAM address 0 into the address counter, and returns the display to its original status if it was shifted. The DDRAM contents do not change.

The cursor or blinking go to the left edge of the display (in the first line if 2 lines are displayed).

Entry Mode Set

I/D: Increments (I/D = 1) or decrements (I/D = 0) the DDRAM address by 1 when a character code is written into or read from DDRAM.

The cursor or blinking moves to the right when incremented by 1 and to the left when decremented by 1. The same applies to writing and reading of CGRAM.

S: Shifts the entire display either to the right (I/D = 0) or to the left (I/D = 1) when S is 1. The display does not shift if S is 0.

If S is 1, it will seem as if the cursor does not move but the display does. The display does not shift when reading from DDRAM. Also, writing into or reading out from CGRAM does not shift the display.

Display On/Off Control

D: The display is on when D is 1 and off when D is 0. When off, the display data remains in DDRAM, but can be displayed instantly by setting D to 1.

C: The cursor is displayed when C is 1 and not displayed when C is 0. Even if the cursor disappears, the function of I/D or other specifications will not change during display data write. The cursor is displayed using 5 dots in the 8th line for 5×8 dot character font selection and in the 11th line for the 5×10 dot character font selection (Figure 13).

B: The character indicated by the cursor blinks when B is 1 (Figure 13). The blinking is displayed as switching between all blank dots and displayed characters at a speed of 409.6-ms intervals when f_{cp} or f_{OSC} is 250 kHz. The cursor and blinking can be set to display simultaneously. (The blinking frequency changes according to f_{OSC} or the reciprocal of f_{cp}. For example, when f_{cp} is 270 kHz, $409.6 \times 250/270 = 379.2$ ms.)

Cursor or Display Shift

Cursor or display shift shifts the cursor position or display to the right or left without writing or reading display data (Table 7). This function is used to correct or search the display. In a 2-line display, the cursor moves to the second line when it passes the 40th digit of the first line. Note that the first and second line displays will shift at the same time.

When the displayed data is shifted repeatedly each line moves only horizontally. The second line display does not shift into the first line position.

The address counter (AC) contents will not change if the only action performed is a display shift.

Function Set

DL: Sets the interface data length. Data is sent or received in 8-bit lengths (DB7 to DB0) when DL is 1, and in 4-bit lengths (DB7 to DB4) when DL is 0.When 4-bit length is selected, data must be sent or received twice.

N: Sets the number of display lines.

F: Sets the character font.

Note: Perform the function at the head of the program before executing any instructions (except for the read busy flag and address instruction). From this point, the function set instruction cannot be executed unless the interface data length is changed.

Set CGRAM Address

Set CGRAM address sets the CGRAM address binary AAAAAA into the address counter.

Data is then written to or read from the MPU for CGRAM.

		RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Clear display	Code	0	0	0	0	0	0	0	0	0	1
Return home	Code	0	0	0	0	0	0	0	0	0	1
Entry mode set	Code	0	0	0	0	0	0	0	0	0	1
Display on/off control	Code	0	0	0	0	0	0	0	0	0	1

Note: * Don't care.

Figure 11

		RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Cursor or display shift	Code	0	0	0	0	0	1	S/C	R/L	*	*
Function set	Code	0	0	0	0	0	DL	N	F	*	*
Set CGRAM address	Code	0	0	0	0	A	A	A	A	A	A

Note: * Don't care.

← Higher order bit　　Lower order bit →

Figure 12

Set DDRAM Address

Set DDRAM address sets the DDRAM address binary AAAAAAA into the address counter.

Data is then written to or read from the MPU for DDRAM.

However, when N is 0 (1-line display), AAAAAAA can be 00H to 4FH. When N is 1 (2-line display), AAAAAAA can be 00H to 27H for the first line, and 40H to 67H for the second line.

Read Busy Flag and Address

Read busy flag and address reads the busy flag (BF) indicating that the system is now internally operating on a previously received instruction. If BF is 1, the internal operation is in progress. The next instruction will not be accepted until BF is reset to 0. Check the BF status before the next write operation. At the same time, the value of the address counter in binary AAAAAAA is read out. This address counter is used by both CG and DDRAM addresses, and its value is determined by the previous instruction. The address contents are the same as for instructions set CGRAM address and set DDRAM address.

Table 7 Shift Function

S/C	R/L	
0	0	Shifts the cursor position to the left. (AC is decremented by one.)
0	1	Shifts the cursor position to the right. (AC is incremented by one.)
1	0	Shifts the entire display to the left. The cursor follows the display shift.
1	1	Shifts the entire display to the right. The cursor follows the display shift.

Table 8 Function Set

N	F	No. of Display Lines	Character Font	Duty Factor	Remarks
0	0	1	5 × 8 dots	1/8	
0	1	1	5 × 10 dots	1/11	
1	*	2	5 × 8 dots	1/16	Cannot display two lines for 5 × 10 dot character font

Note: * Indicates don’t care.

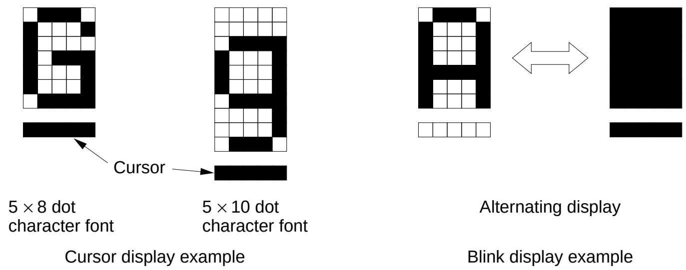


Figure 13   Cursor and Blinking

Set DDRAM address

	RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	1	A	A	A	A	A	A	A

← Higher order bit … Lower order bit →

Read busy flag and address

	RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	1	BF	A	A	A	A	A	A	A

← Higher order bit … Lower order bit →

Figure 14

Write Data to CG or DDRAM

Write data to CG or DDRAM writes 8-bit binary data DDDDDDDD to CG or DDRAM.

To write into CG or DDRAM is determined by the previous specification of the CGRAM or DDRAM address setting. After a write, the address is automatically incremented or decremented by 1 according to the entry mode. The entry mode also determines the display shift.

Read Data from CG or DDRAM

Read data from CG or DDRAM reads 8-bit binary data DDDDDDDD from CG or DDRAM.

The previous designation determines whether CG or DDRAM is to be read. Before entering this read instruction, either CGRAM or DDRAM address set instruction must be executed. If not executed, the first read data will be invalid. When serially executing read instructions, the next address data is normally read from the second read. The address set instructions need not be executed just before this read instruction when shifting the cursor by the cursor shift instruction (when reading out DDRAM). The operation of the cursor shift instruction is the same as the set DDRAM address instruction.

After a read, the entry mode automatically increases or decreases the address by 1. However, display shift is not executed regardless of the entry mode.

Note: The address counter (AC) is automatically incremented or decremented by 1 after the write instructions to CGRAM or DDRAM are executed. The RAM data selected by the AC cannot be read out at this time even if read instructions are executed. Therefore, to correctly read data, execute either the address set instruction or cursor shift instruction (only with DDRAM), then just before reading the desired data, execute the read instruction from the second time the read instruction is sent.

Write data to CG or DDRAM		RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
	Code	1	0	D	D	D	D	D	D	D	D

← Higher order bits   Lower order bits →

Read data from CG or DDRAM		RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
	Code	1	1	D	D	D	D	D	D	D	D

← Higher order bits   Lower order bits →

Figure 15

Interfacing the HD44780U

Interface to MPUs

- Interfacing to an 8-bit MPU

  See Figure 17 for an example of using a I/O port (for a single-chip microcomputer) as an interface device.

  In this example, P30 to P37 are connected to the data bus DB0 to DB7, and P75 to P77 are connected to E, R/$\overline{W}$, and RS, respectively.

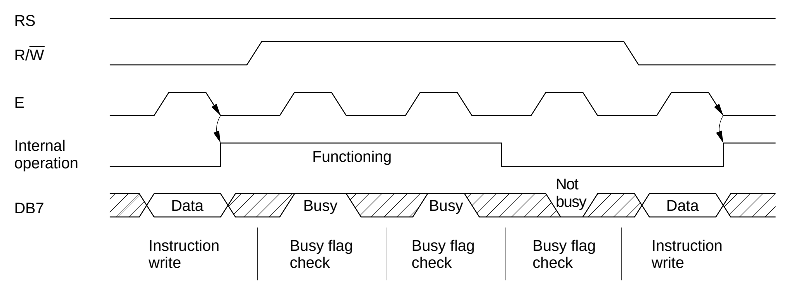


Figure 16 Example of Busy Flag Check Timing Sequence

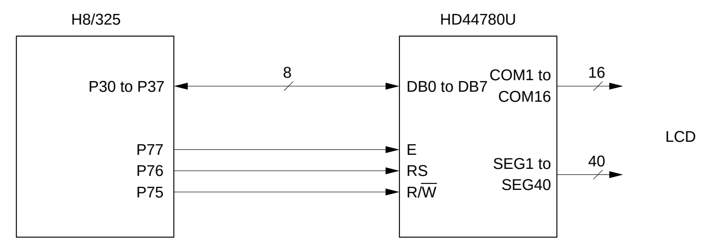


Figure 17 H8/325 Interface (Single-Chip Mode)

- Interfacing to a 4-bit MPU

  The HD44780U can be connected to the I/O port of a 4-bit MPU. If the I/O port has enough bits, 8-bit data can be transferred. Otherwise, one data transfer must be made in two operations for 4-bit data. In this case, the timing sequence becomes somewhat complex. (See Figure 18.)

  See Figure 19 for an interface example to the HMCS4019R.

  Note that two cycles are needed for the busy flag check as well as for the data transfer. The 4-bit operation is selected by the program.

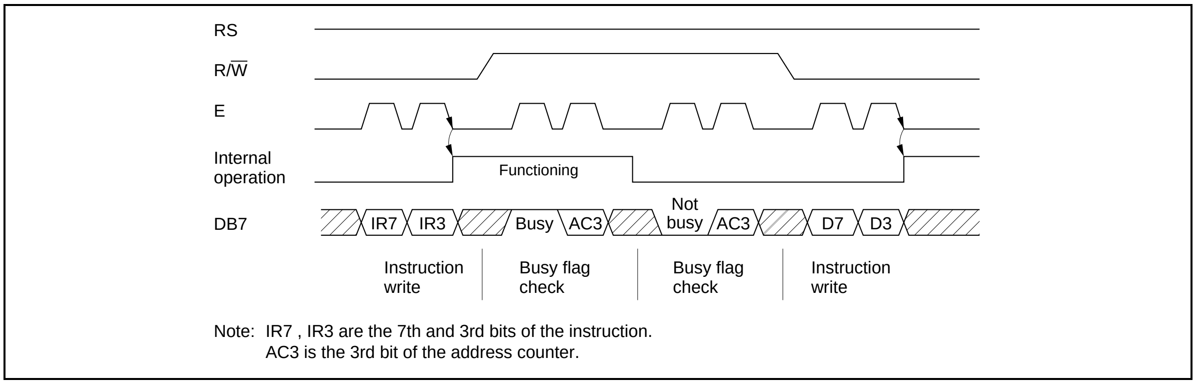


Figure 18 Example of 4-Bit Data Transfer Timing Sequence

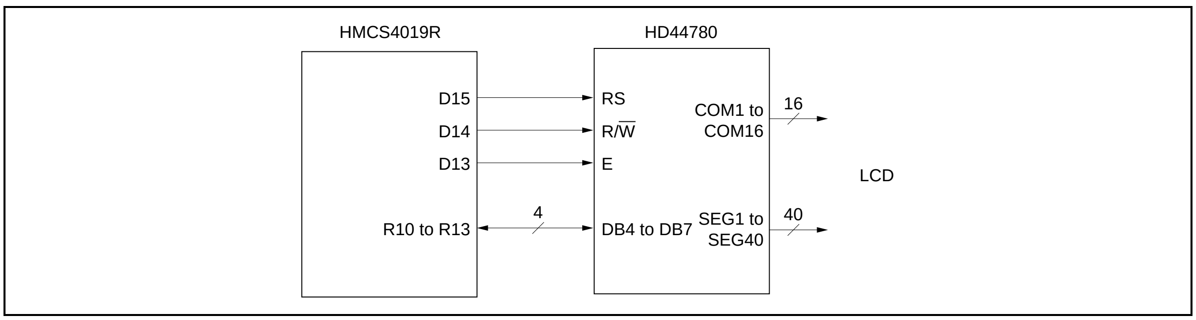


Figure 19 Example of Interface to HMCS4019R

Interface to Liquid Crystal Display

Character Font and Number of Lines: The HD44780U can perform two types of displays, 5 × 8 dot and 5 × 10 dot character fonts, each with a cursor.

Up to two lines are displayed for 5 × 8 dots and one line for 5 × 10 dots. Therefore, a total of three

types of common signals are available (Table 9).

The number of lines and font types can be selected by the program. (See Table 6, Instructions.)

Connection to HD44780 and Liquid Crystal Display: See Figure 20 for the connection examples.

Table 9 Common Signals

Number of Lines	Character Font	Number of Common Signals	Duty Factor
1	5 × 8 dots + cursor	8	1/8
1	5 × 10 dots + cursor	11	1/11
2	5 × 8 dots + cursor	16	1/16

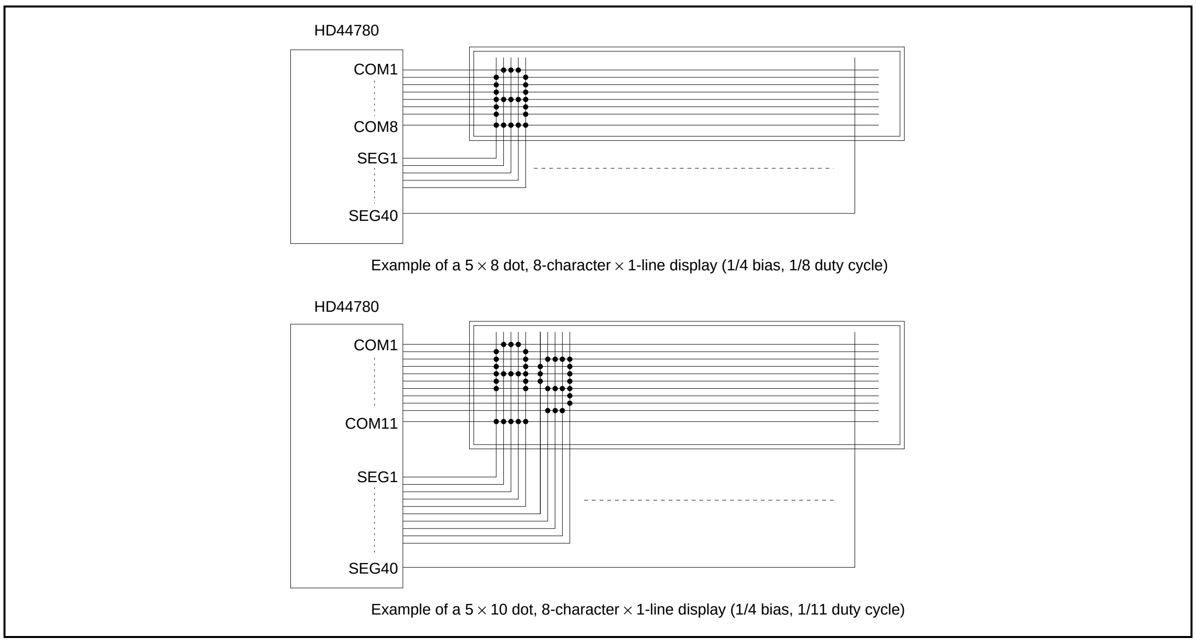


Figure 20 Liquid Crystal Display and HD44780 Connections

Since five segment signal lines can display one digit, one HD44780U can display up to 8 digits for a 1-line display and 16 digits for a 2-line display.

The examples in Figure 20 have unused common signal pins, which always output non-selection waveforms. When the liquid crystal display panel has unused extra scanning lines, connect the extra scanning lines to these common signal pins to avoid any undesirable effects due to crosstalk during the floating state (Figure 21).

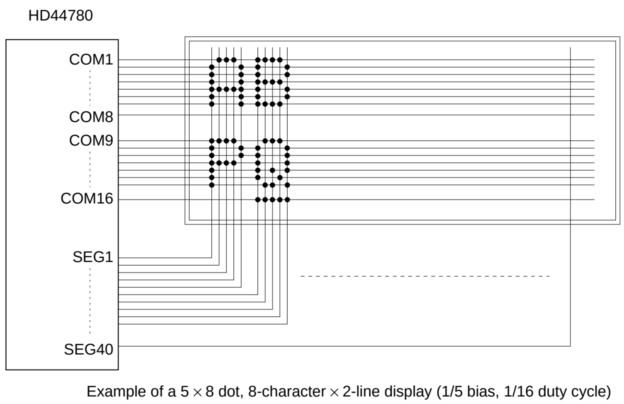


Figure 20 Liquid Crystal Display and HD44780 Connections (cont)

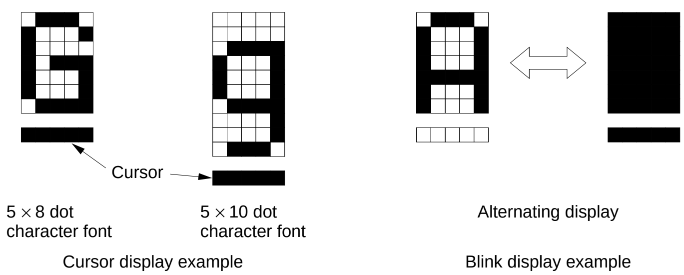


Figure 21 Using COM9 to Avoid Crosstalk on Unneeded Scanning Line

Connection of Changed Matrix Layout: In the preceding examples, the number of lines correspond to the scanning lines. However, the following display examples (Figure 22) are made possible by altering the matrix layout of the liquid crystal display panel. In either case, the only change is the layout. The display characteristics and the number of liquid crystal display characters depend on the number of common signals or on duty factor. Note that the display data RAM (DDRAM) addresses for 4 characters × 2 lines and for 16 characters × 1 line are the same as in Figure 20.

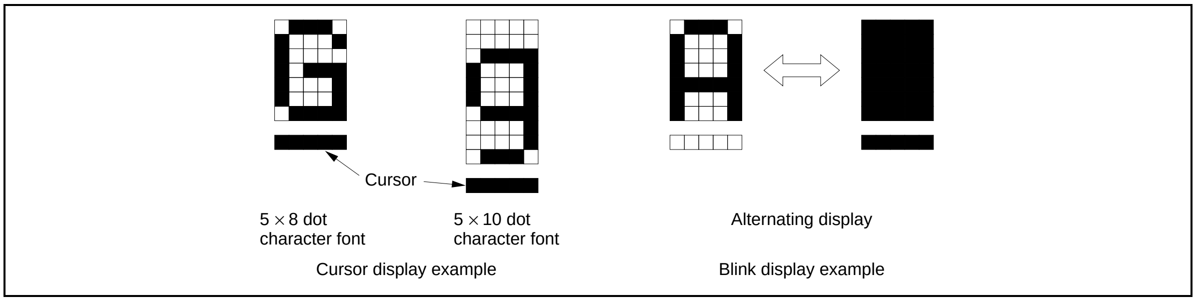


Figure 22 Changed Matrix Layout Displays

Power Supply for Liquid Crystal Display Drive

Various voltage levels must be applied to pins V1 to V5 of the HD44780U to obtain the liquid crystal display drive waveforms. The voltages must be changed according to the duty factor (Table 10).

VLCD is the peak value for the liquid crystal display drive waveforms, and resistance dividing provides voltages V1 to V5 (Figure 23).

Table 10 Duty Factor and Power Supply for Liquid Crystal Display Drive

	Duty Factor	
	1/8, 1/11	**1/16**
	Bias	
Power Supply	**1/4**	**1/5**
V1	V_{cc}–1/4 VLCD	V_{cc}–1/5 VLCD
V2	V_{cc}–1/2 VLCD	V_{cc}–2/5 VLCD
V3	V_{cc}–1/2 VLCD	V_{cc}–3/5 VLCD
V4	V_{cc}–3/4 VLCD	V_{cc}–4/5 VLCD
V5	V_{cc}–VLCD	V_{cc}–VLCD

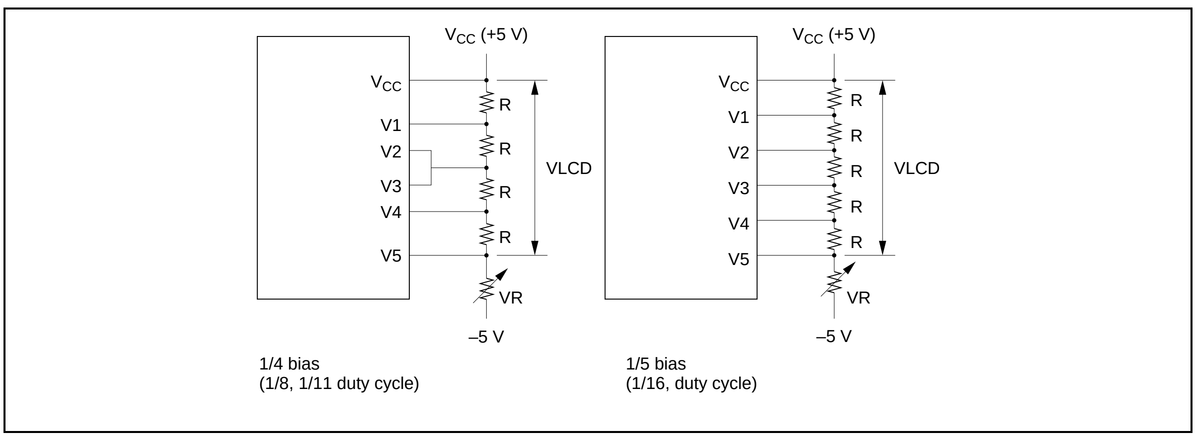
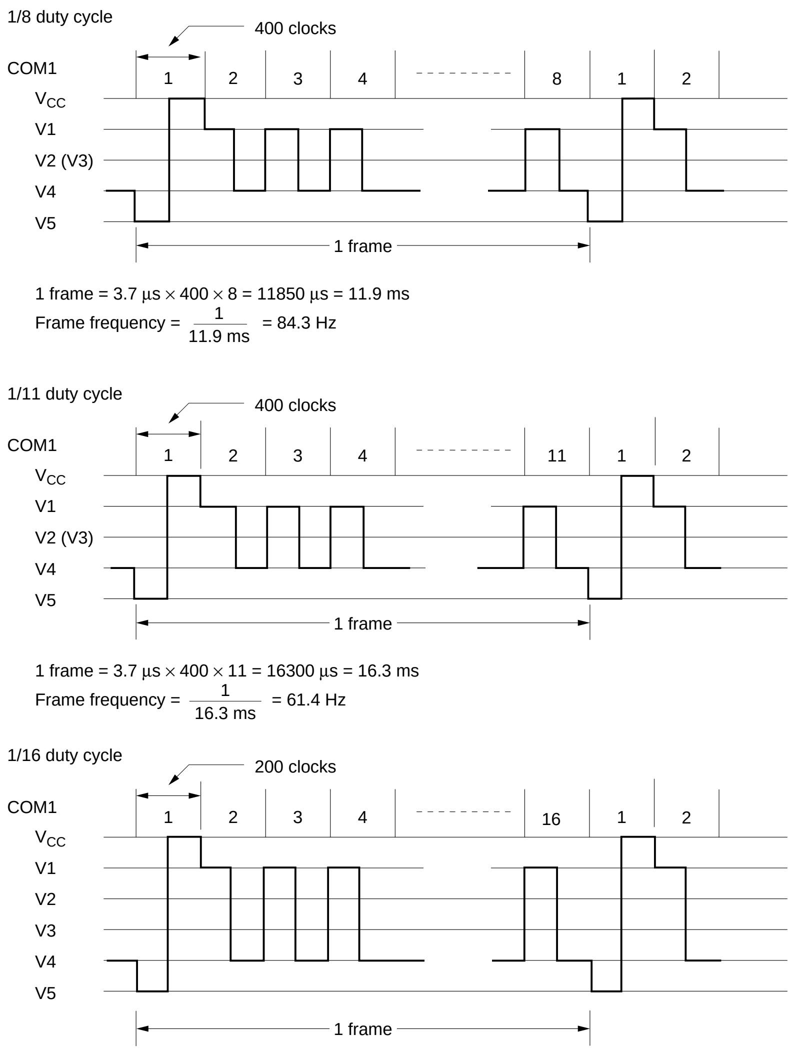


Figure 23 Drive Voltage Supply Example

Relationship between Oscillation Frequency and Liquid Crystal Display Frame Frequency

The liquid crystal display frame frequencies of Figure 24 apply only when the oscillation frequency is 270 kHz (one clock pulse of 3.7 µs).



1 frame = 3.7 µs × 400 × 8 = 11850 µs = 11.9 ms

Frame frequency = $\frac{1}{11.9\ \text{ms}}$ = 84.3 Hz

1 frame = 3.7 µs × 400 × 11 = 16300 µs = 16.3 ms

Frame frequency = $\frac{1}{16.3\ \text{ms}}$ = 61.4 Hz

1 frame = 3.7 µs × 200 × 16 = 11850 µs = 11.9 ms

Frame frequency = $\frac{1}{11.9\ \text{ms}}$ = 84.3 Hz

Figure 24 Frame Frequency

Instruction and Display Correspondence

- 8-bit operation, 8-digit × 1-line display with internal reset

  Refer to Table 11 for an example of an 8-digit × 1-line display in 8-bit operation. The HD44780U functions must be set by the function set instruction prior to the display. Since the display data RAM can store data for 80 characters, as explained before, the RAM can be used for displays such as for advertising when combined with the display shift operation.

  Since the display shift operation changes only the display position with DDRAM contents unchanged, the first display data entered into DDRAM can be output when the return home operation is performed.

- 4-bit operation, 8-digit × 1-line display with internal reset

  The program must set all functions prior to the 4-bit operation (Table 12). When the power is turned on, 8-bit operation is automatically selected and the first write is performed as an 8-bit operation. Since DB0 to DB3 are not connected, a rewrite is then required. However, since one operation is completed in two accesses for 4-bit operation, a rewrite is needed to set the functions (see Table 12). Thus, DB4 to DB7 of the function set instruction is written twice.

- 8-bit operation, 8-digit × 2-line display

  For a 2-line display, the cursor automatically moves from the first to the second line after the 40th digit of the first line has been written. Thus, if there are only 8 characters in the first line, the DDRAM address must be again set after the 8th character is completed. (See Table 13.) Note that the display shift operation is performed for the first and second lines. In the example of Table 13, the display shift is performed when the cursor is on the second line. However, if the shift operation is performed when the cursor is on the first line, both the first and second lines move together. If the shift is repeated, the display of the second line will not move to the first line. The same display will only shift within its own line for the number of times the shift is repeated.

Note: When using the internal reset, the electrical characteristics in the Power Supply Conditions Using Internal Reset Circuit table must be satisfied. If not, the HD44780U must be initialized by instructions. See the section, Initializing by Instruction.

Table 11 8-Bit Operation, 8-Digit × 1-Line Display Example with Internal Reset

Step No.	RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Display	Operation
1	Power supply on (the HD44780U is initialized by the internal reset circuit)											Initialized. No display.
2	Function set 0	0	0	0	1	1	0	0	*	*		Sets to 8-bit operation and selects 1-line display and 5 × 8 dot character font. (Number of display lines and character fonts cannot be changed after step #2.)
3	Display on/off control 0	0	0	0	0	0	1	1	1	0	_	Turns on display and cursor. Entire display is in space mode because of initialization.
4	Entry mode set 0	0	0	0	0	0	0	1	1	0	_	Sets mode to increment the address by one and to shift the cursor to the right at the time of write to the DD/CGRAM. Display is not shifted.
5	Write data to CGRAM/DDRAM 1	0	0	1	0	0	1	0	0	0	H_	Writes H. DDRAM has already been selected by initialization when the power was turned on. The cursor is incremented by one and shifted to the right.
6	Write data to CGRAM/DDRAM 1	0	0	1	0	0	1	0	0	1	HI_	Writes I.
7						⋮					⋮	
8	Write data to CGRAM/DDRAM 1	0	0	1	0	0	1	0	0	1	HITACHI_	Writes I.
9	Entry mode set 0	0	0	0	0	0	0	1	1	1	HITACHI_	Sets mode to shift display at the time of write.
10	Write data to CGRAM/DDRAM 1	0	0	0	1	0	0	0	0	0	ITACHI _	Writes a space.

Table 11 8-Bit Operation, 8-Digit × 1-Line Display Example with Internal Reset (cont)

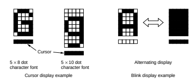
Step No.	Instruction										Display	Operation
	RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
11	Write data to CGRAM/DDRAM											Writes M.
	1	0	0	1	0	0	1	1	0	1		
12	. . . . .										. . . . .	
13	Write data to CGRAM/DDRAM										MICROKO_	Writes O.
	1	0	0	1	0	0	1	1	1	1		
14	Cursor or display shift										MICROKO	Shifts only the cursor position to the left.
	0	0	0	0	0	1	0	0	*	*		
15	Cursor or display shift										MICROKO	Shifts only the cursor position to the left.
	0	0	0	0	0	1	0	0	*	*		
16	Write data to CGRAM/DDRAM										ICROCO	Writes C over K. The display moves to the left.
	1	0	0	1	0	0	0	0	1	1		
17	Cursor or display shift										MICROCO	Shifts the display and cursor position to the right.
	0	0	0	0	0	1	1	1	*	*		
18	Cursor or display shift										MICROCO_	Shifts the display and cursor position to the right.
	0	0	0	0	0	1	0	1	*	*		
19	Write data to CGRAM/DDRAM										ICROCOM_	Writes M.
	1	0	0	1	0	0	1	1	0	1		
20	. . . . .										. . . . .	
21	Return home										HITACHI	Returns both display and cursor to the original position (address 0).
	0	0	0	0	0	0	0	0	1	0		

Table 12 4-Bit Operation, 8-Digit × 1-Line Display Example with Internal Reset

Step	Instruction							
No.	RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	Display	Operation
1	Power supply on (the HD44780U is initialized by the internal reset circuit)							Initialized. No display.
2	Function set 0	 0	 0	 0	 1	 0		Sets to 4-bit operation. In this case, operation is handled as 8 bits by initialization, and only this instruction completes with one write.
3	Function set 0 0	 0 0	 0 0	 0 0	 1 *	 0 *		Sets 4-bit operation and selects 1-line display and 5 × 8 dot character font. 4-bit operation starts from this step and resetting is necessary. (Number of display lines and character fonts cannot be changed after step #3.)
4	Display on/off control 0 0	 0 0	 0 1	 0 1	 0 1	 0 0	_	Turns on display and cursor. Entire display is in space mode because of initialization.
5	Entry mode set 0 0	 0 0	 0 0	 0 1	 0 1	 0 0	_	Sets mode to increment the address by one and to shift the cursor to the right at the time of write to the DD/CGRAM. Display is not shifted.
6	Write data to CGRAM/DDRAM 1 1	 0 0	 0 1	 1 0	 0 0	 0 0	H_	Writes H. The cursor is incremented by one and shifts to the right.

Note: The control is the same as for 8-bit operation beyond step #6.

Table 13 8-Bit Operation, 8-Digit × 2-Line Display Example with Internal Reset

Step	Instruction											
No.	**RS**	**$R/\overline{W}$**	**DB7**	**DB6**	**DB5**	**DB4**	**DB3**	**DB2**	**DB1**	**DB0**	**Display**	**Operation**
1	Power supply on (the HD44780U is initialized by the internal reset circuit)											Initialized. No display.
2	Function set											Sets to 8-bit operation and selects 2-line display and 5 × 8 dot character font.
	0	0	0	0	1	1	1	0	*	*		
3	Display on/off control										_	Turns on display and cursor. All display is in space mode because of initialization.
	0	0	0	0	0	0	1	1	1	0		
4	Entry mode set										_	Sets mode to increment the address by one and to shift the cursor to the right at the time of write to the DD/CGRAM. Display is not shifted.
	0	0	0	0	0	0	0	1	1	0		
5	Write data to CGRAM/DDRAM										H_	Writes H. DDRAM has already been selected by initialization when the power was turned on. The cursor is incremented by one and shifted to the right.
	1	0	0	1	0	0	1	0	0	0		
6						. . . . .					. . . . .	
7	Write data to CGRAM/DDRAM										HITACHI_	Writes I.
	1	0	0	1	0	0	1	0	0	1		
8	Set DDRAM address										HITACHI _	Sets DDRAM address so that the cursor is positioned at the head of the second line.
	0	0	1	1	0	0	0	0	0	0		

Table 13 8-Bit Operation, 8-Digit × 2-Line Display Example with Internal Reset (cont)

Step No.	Instruction RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Display	Operation
9	Write data to CGRAM/DDRAM										HITACHI M_	Writes M.
	1	0	0	1	0	0	1	1	0	1		
10						. . . . .					. . . . .	
11	Write data to CGRAM/DDRAM										HITACHI MICROCO_	Writes O.
	1	0	0	1	0	0	1	1	1	1		
12	Entry mode set										HITACHI MICROCO_	Sets mode to shift display at the time of write.
	0	0	0	0	0	0	0	1	1	1		
13	Write data to CGRAM/DDRAM										ITACHI ICROCOM_	Writes M. Display is shifted to the left. The first and second lines both shift at the same time.
	1	0	0	1	0	0	1	1	0	1		
14						. . . . .					. . . . .	
15	Return home										HITACHI MICROCOM	Returns both display and cursor to the original position (address 0).
	0	0	0	0	0	0	0	0	1	0		

Initializing by Instruction

If the power supply conditions for correctly operating the internal reset circuit are not met, initialization by instructions becomes necessary.

Refer to Figures 25 and 26 for the procedures on 8-bit and 4-bit initializations, respectively.

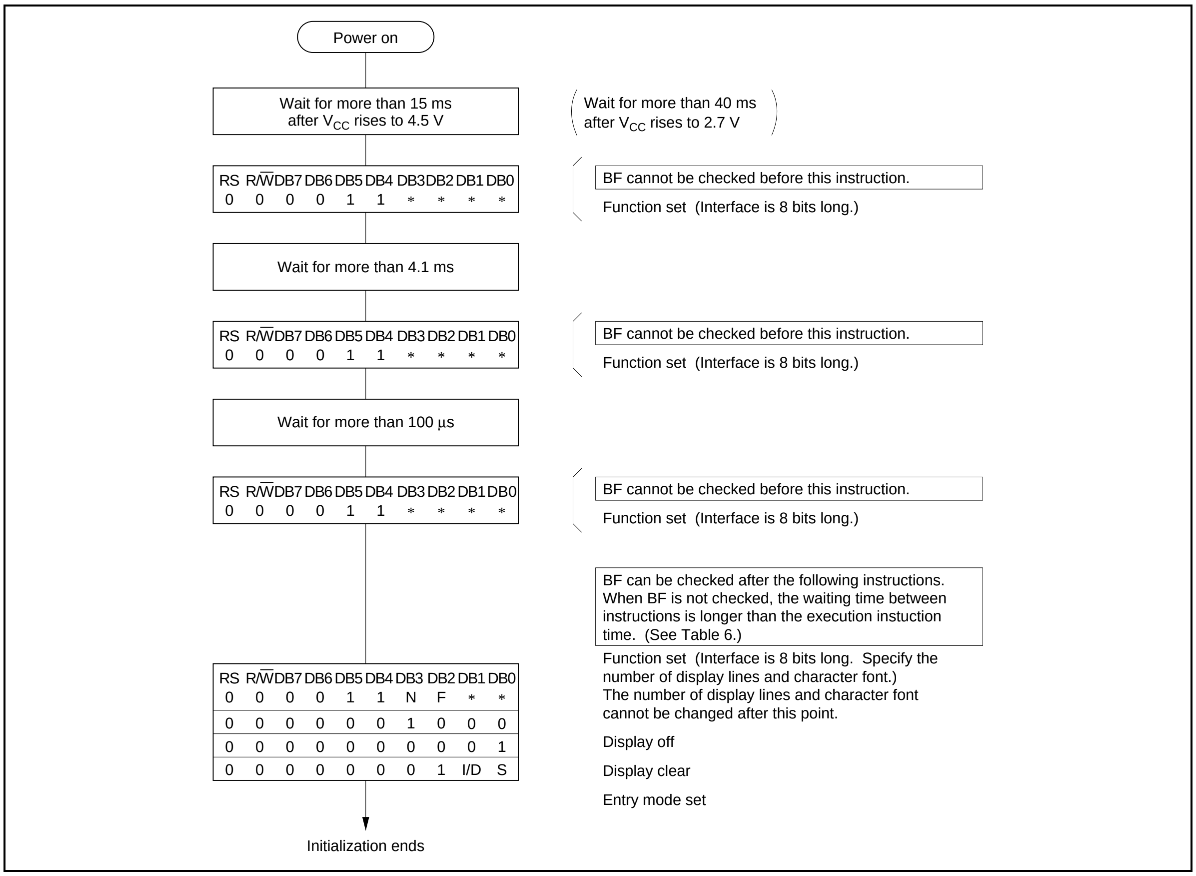


Figure 25 8-Bit Interface

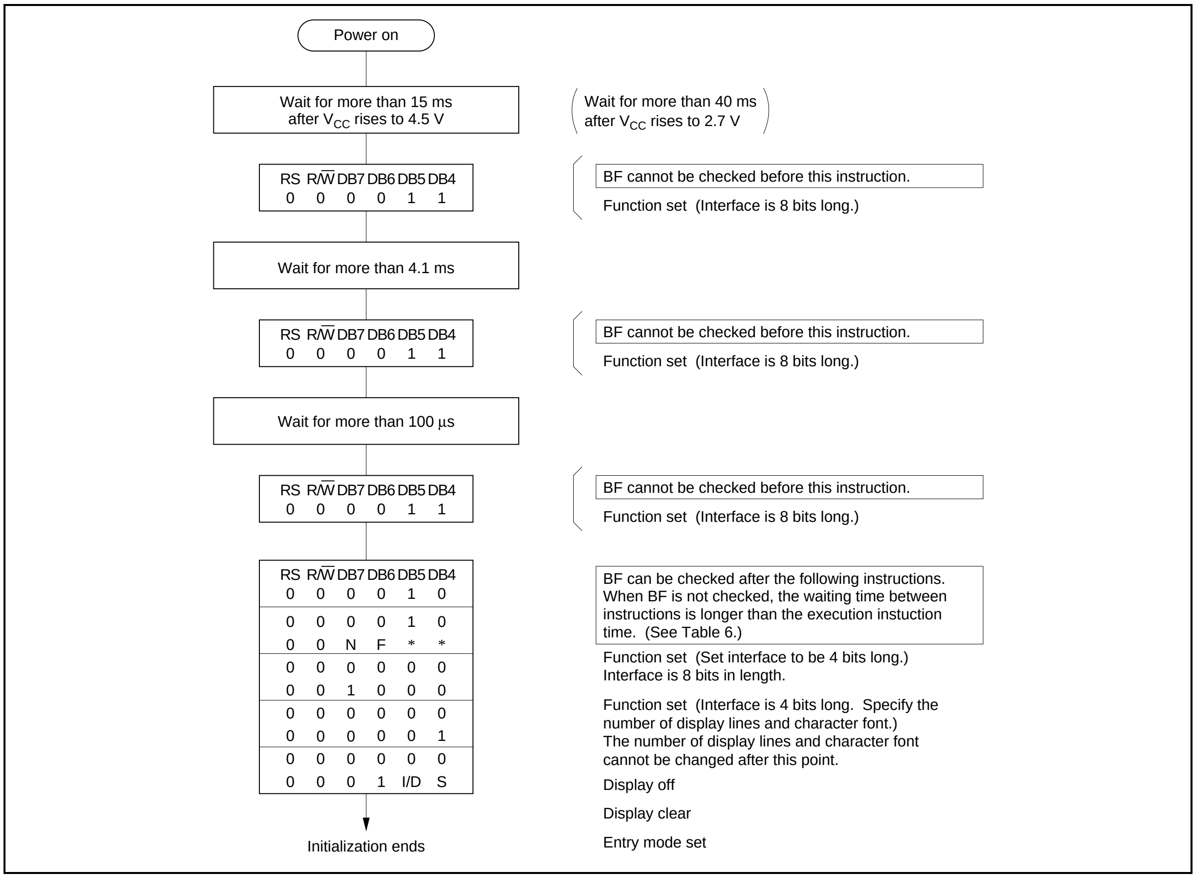


Figure 26 4-Bit Interface

Absolute Maximum Ratings*

Item	Symbol	Value	Unit	Notes
Power supply voltage (1)	V_{CC}–GND	–0.3 to +7.0	V	1
Power supply voltage (2)	V_{CC}–V5	–0.3 to +13.0	V	1, 2
Input voltage	Vt	–0.3 to V_{CC} +0.3	V	1
Operating temperature	T_{opr}	–20 to +75	°C	
Storage temperature	T_{stg}	–55 to +125	°C	4

Note: * If the LSI is used above these absolute maximum ratings, it may become permanently damaged. Using the LSI within the following electrical characteristic limits is strongly recommended for normal operation. If these electrical characteristic conditions are also exceeded, the LSI will malfunction and cause poor reliability.

DC Characteristics (V_{CC} = 2.7 to 4.5 V, T_a = –20 to +75°C*[3])

Item	Symbol	Min	Typ	Max	Unit	Test Condition	Notes*
Input high voltage (1) (except OSC1)	VIH1	$0.7V_{CC}$	—	V_{CC}	V		6
Input low voltage (1) (except OSC1)	VIL1	–0.3	—	0.55	V		6
Input high voltage (2) (OSC1)	VIH2	$0.7V_{CC}$	—	V_{CC}	V		15
Input low voltage (2) (OSC1)	VIL2	—	—	$0.2V_{CC}$	V		15
Output high voltage (1) (DB0–DB7)	VOH1	$0.75V_{CC}$	—	—	V	$-I_{OH}$ = 0.1 mA	7
Output low voltage (1) (DB0–DB7)	VOL1	—	—	$0.2V_{CC}$	V	I_{OL} = 0.1 mA	7
Output high voltage (2) (except DB0–DB7)	VOH2	$0.8V_{CC}$	—	—	V	$-I_{OH}$ = 0.04 mA	8
Output low voltage (2) (except DB0–DB7)	VOL2	—	—	$0.2V_{CC}$	V	I_{OL} = 0.04 mA	8
Driver on resistance (COM)	R_{COM}	—	2	20	kΩ	±Id = 0.05 mA, VLCD = 4 V	13
Driver on resistance (SEG)	R_{SEG}	—	2	30	kΩ	±Id = 0.05 mA, VLCD = 4 V	13
Input leakage current	I_{LI}	–1	—	1	µA	VIN = 0 to V_{CC}	9
Pull-up MOS current (DB0–DB7, RS, R/$\overline{W}$)	$-I_p$	10	50	120	µA	V_{CC} = 3 V	
Power supply current	I_{CC}	—	0.15	0.30	mA	R_f oscillation, external clock V_{CC} = 3 V, f_{OSC} = 270 kHz	10, 14
LCD voltage	VLCD1	3.0	—	11.0	V	V_{CC}–V5, 1/5 bias	16
	VLCD2	3.0	—	11.0	V	V_{CC}–V5, 1/4 bias	16

Note: * Refer to the Electrical Characteristics Notes section following these tables.

AC Characteristics (V_{CC} = 2.7 to 4.5 V, T_a = –20 to +75°C*[3])

Clock Characteristics

Item		Symbol	Min	Typ	Max	Unit	Test Condition	Note*
External clock operation	External clock frequency	f_{cp}	125	250	350	kHz		11
	External clock duty	Duty	45	50	55	%		
	External clock rise time	t_{rcp}	—	—	0.2	µs		
	External clock fall time	t_{fcp}	—	—	0.2	µs		
R_f oscillation	Clock oscillation frequency	f_{OSC}	190	270	350	kHz	R_f = 75 kΩ, V_{CC} = 3 V	12

Note: * Refer to the Electrical Characteristics Notes section following these tables.

Bus Timing Characteristics

Write Operation

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Enable cycle time	t_{cycE}	1000	—	—	ns	Figure 27
Enable pulse width (high level)	PW_{EH}	450	—	—		
Enable rise/fall time	t_{Er}, t_{Ef}	—	—	25		
Address set-up time (RS, R/$\overline{W}$ to E)	t_{AS}	60	—	—		
Address hold time	t_{AH}	20	—	—		
Data set-up time	t_{DSW}	195	—	—		
Data hold time	t_H	10	—	—		

Read Operation

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Enable cycle time	t_{cycE}	1000	—	—	ns	Figure 28
Enable pulse width (high level)	PW_{EH}	450	—	—		
Enable rise/fall time	t_{Er}, t_{Ef}	—	—	25		
Address set-up time (RS, R/$\overline{W}$ to E)	t_{AS}	60	—	—		
Address hold time	t_{AH}	20	—	—		
Data delay time	t_{DDR}	—	—	360		
Data hold time	t_{DHR}	5	—	—		

Interface Timing Characteristics with External Driver

Item		Symbol	Min	Typ	Max	Unit	Test Condition
Clock pulse width	High level	t_{CWH}	800	—	—	ns	Figure 29
	Low level	t_{CWL}	800	—	—		
Clock set-up time		t_{CSU}	500	—	—		
Data set-up time		t_{SU}	300	—	—		
Data hold time		t_{DH}	300	—	—		
M delay time		t_{DM}	–1000	—	1000		
Clock rise/fall time		t_{ct}	—	—	200		

Power Supply Conditions Using Internal Reset Circuit

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Power supply rise time	t_{rCC}	0.1	—	10	ms	Figure 30
Power supply off time	t_{OFF}	1	—	—		

DC Characteristics (V_{CC} = 4.5 to 5.5 V, T_a = –20 to +75°C*[3])

Item	Symbol	Min	Typ	Max	Unit	Test Condition	Notes*
Input high voltage (1) (except OSC1)	VIH1	2.2	—	V_{CC}	V		6
Input low voltage (1) (except OSC1)	VIL1	–0.3	—	0.6	V		6
Input high voltage (2) (OSC1)	VIH2	V_{CC}–1.0	—	V_{CC}	V		15
Input low voltage (2) (OSC1)	VIL2	—	—	1.0	V		15
Output high voltage (1) (DB0–DB7)	VOH1	2.4	—	—	V	$–I_{OH}$ = 0.205 mA	7
Output low voltage (1) (DB0–DB7)	VOL1	—	—	0.4	V	I_{OL} = 1.2 mA	7
Output high voltage (2) (except DB0–DB7)	VOH2	0.9 V_{CC}	—	—	V	$–I_{OH}$ = 0.04 mA	8
Output low voltage (2) (except DB0–DB7)	VOL2	—	—	0.1 V_{CC}	V	I_{OL} = 0.04 mA	8
Driver on resistance (COM)	RCOM	—	2	20	kΩ	±Id = 0.05 mA, VLCD = 4 V	13
Driver on resistance (SEG)	RSEG	—	2	30	kΩ	±Id = 0.05 mA, VLCD = 4 V	13
Input leakage current	I_{LI}	–1	—	1	µA	VIN = 0 to V_{CC}	9
Pull-up MOS current (DB0–DB7, RS, R/$\overline{W}$)	$–I_p$	50	125	250	µA	V_{CC} = 5 V	
Power supply current	I_{CC}	—	0.35	0.60	mA	R_f oscillation, external clock V_{CC} = 5 V, f_{OSC} = 270 kHz	10, 14
LCD voltage	VLCD1	3.0	—	11.0	V	V_{CC}–V5, 1/5 bias	16
	VLCD2	3.0	—	11.0	V	V_{CC}–V5, 1/4 bias	16

Note: * Refer to the Electrical Characteristics Notes section following these tables.

AC Characteristics (V_{CC} = 4.5 to 5.5 V, T_a = –20 to +75°C*[3])

Clock Characteristics

Item		Symbol	Min	Typ	Max	Unit	Test Condition	Notes*
External clock operation	External clock frequency	f_{cp}	125	250	350	kHz		11
	External clock duty	Duty	45	50	55	%		11
	External clock rise time	t_{rcp}	—	—	0.2	μs		11
	External clock fall time	t_{fcp}	—	—	0.2	μs		11
R_f oscillation	Clock oscillation frequency	f_{OSC}	190	270	350	kHz	R_f = 91 kΩ V_{CC} = 5.0 V	12

Note: * Refer to the Electrical Characteristics Notes section following these tables.

Bus Timing Characteristics

Write Operation

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Enable cycle time	t_{cycE}	500	—	—	ns	Figure 27
Enable pulse width (high level)	PW_{EH}	230	—	—		
Enable rise/fall time	t_{Er}, t_{Ef}	—	—	20		
Address set-up time (RS, R/$\overline{W}$ to E)	t_{AS}	40	—	—		
Address hold time	t_{AH}	10	—	—		
Data set-up time	t_{DSW}	80	—	—		
Data hold time	t_H	10	—	—		

Read Operation

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Enable cycle time	t_{cycE}	500	—	—	ns	Figure 28
Enable pulse width (high level)	PW_{EH}	230	—	—		
Enable rise/fall time	t_{Er}, t_{Ef}	—	—	20		
Address set-up time (RS, R/$\overline{W}$ to E)	t_{AS}	40	—	—		
Address hold time	t_{AH}	10	—	—		
Data delay time	t_{DDR}	—	—	160		
Data hold time	t_{DHR}	5	—	—		

Interface Timing Characteristics with External Driver

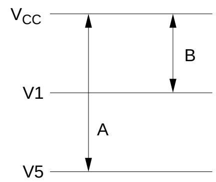
Item		Symbol	Min	Typ	Max	Unit	Test Condition
Clock pulse width	High level	t_{CWH}	800	—	—	ns	Figure 29
	Low level	t_{CWL}	800	—	—		
Clock set-up time		t_{CSU}	500	—	—		
Data set-up time		t_{SU}	300	—	—		
Data hold time		t_{DH}	300	—	—		
M delay time		t_{DM}	–1000	—	1000		
Clock rise/fall time		t_{ct}	—	—	100		

Power Supply Conditions Using Internal Reset Circuit

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Power supply rise time	t_{rCC}	0.1	—	10	ms	Figure 30
Power supply off time	t_{OFF}	1	—	—		

Electrical Characteristics Notes

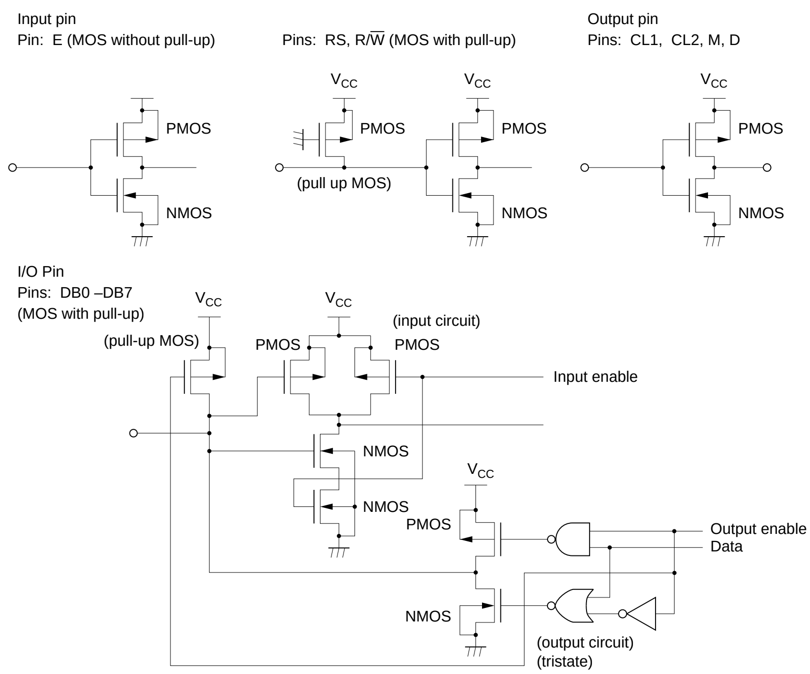
1. All voltage values are referred to GND = 0 V.



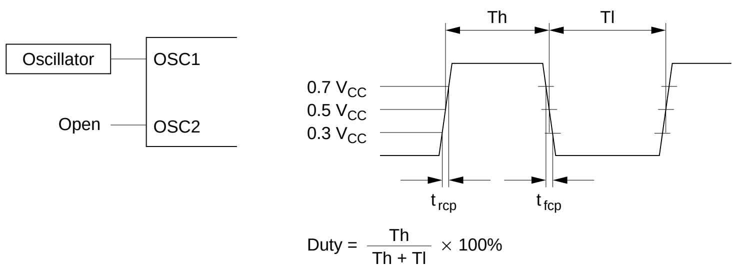
$A = V_{CC} - V5$
$B = V_{CC} - V1$
$A \geq 1.5$ V
$B \leq 0.25 \times A$

The conditions of V1 and V5 voltages are for proper operation of the LSI and not for the LCD output level. The LCD drive voltage condition for the LCD output level is specified as LCD voltage VLCD.

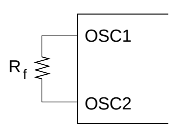
2. $V_{CC} \geq V1 \geq V2 \geq V3 \geq V4 \geq V5$ must be maintained.
3. For die products, specified up to 75°C.
4. For die products, specified by the die shipment specification.
5. The following four circuits are I/O pin configurations except for liquid crystal display output.

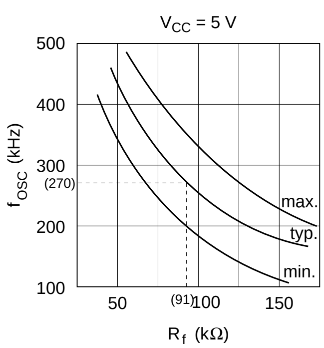


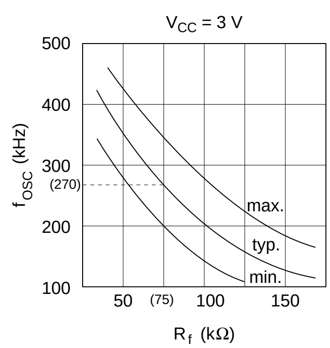
6. Applies to input pins and I/O pins, excluding the OSC1 pin.
7. Applies to I/O pins.
8. Applies to output pins.
9. Current flowing through pull–up MOSs, excluding output drive MOSs.
10. Input/output current is excluded. When input is at an intermediate level with CMOS, the excessive current flows through the input circuit to the power supply. To avoid this from happening, the input level must be fixed high or low.
11. Applies only to external clock operation.



12. Applies only to the internal oscillator operation using oscillation resistor R_f.



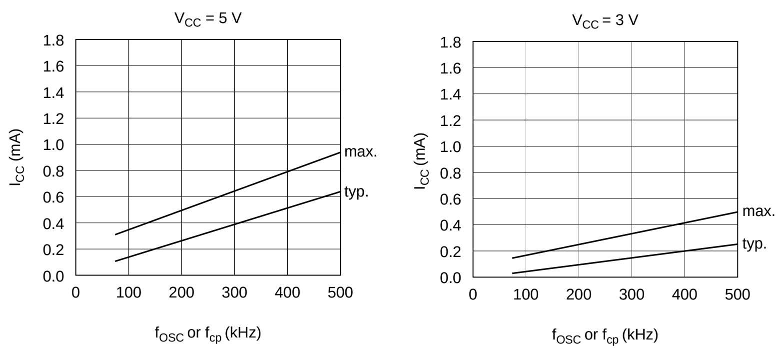




13. RCOM is the resistance between the power supply pins (V_{CC}, V1, V4, V5) and each common signal pin (COM1 to COM16).

    RSEG is the resistance between the power supply pins (V_{CC}, V2, V3, V5) and each segment signal pin (SEG1 to SEG40).

14. The following graphs show the relationship between operation frequency and current consumption.

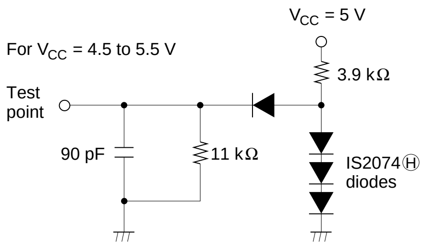


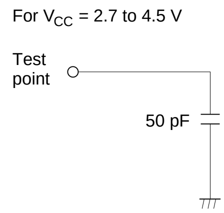
15. Applies to the OSC1 pin.

16. Each COM and SEG output voltage is within ±0.15 V of the LCD voltage (V_{CC}, V1, V2, V3, V4, V5) when there is no load.

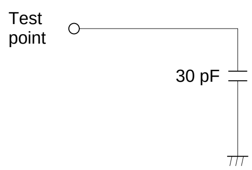
Load Circuits

Data Bus DB0 to DB7





External Driver Control Signals: CL1, CL2, D, M



Timing Characteristics

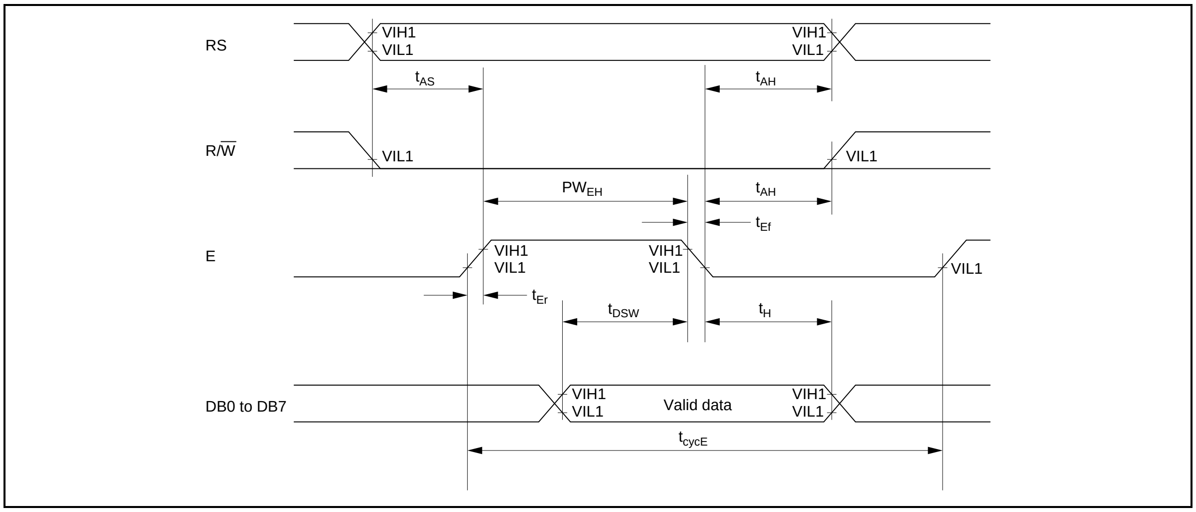


Figure 27 Write Operation

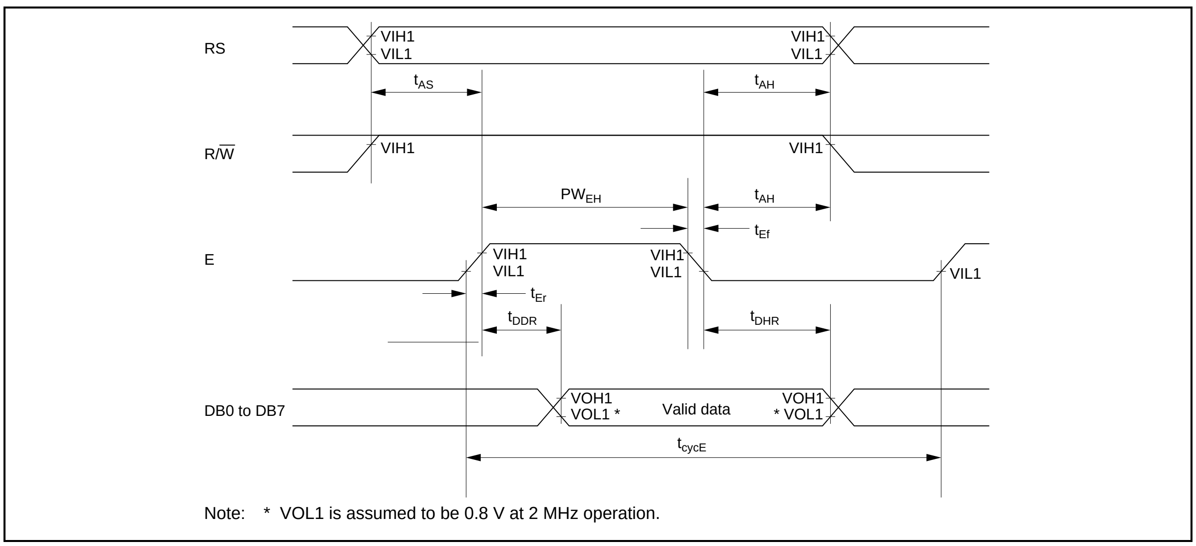


Figure 28 Read Operation

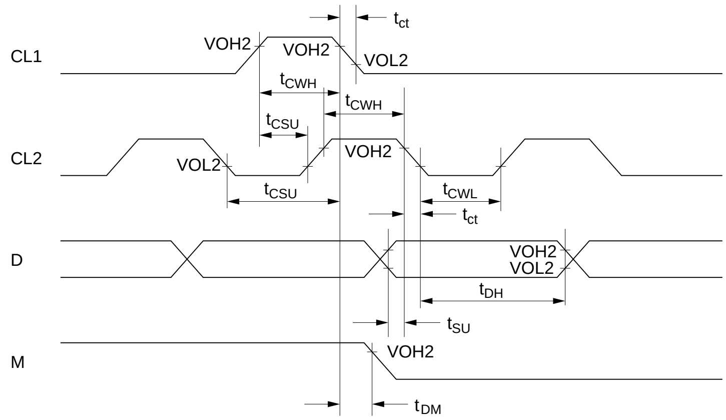
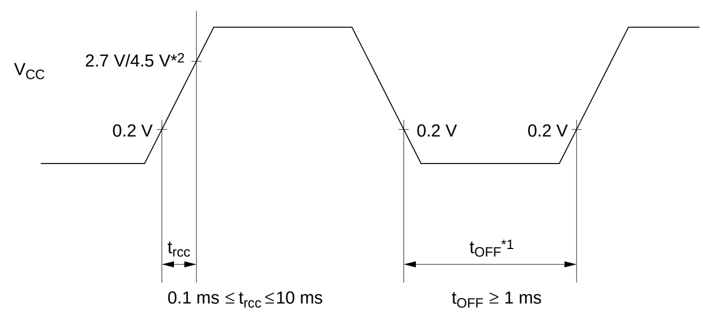


Figure 29 Interface Timing with External Driver



Notes:
1. t_{OFF} compensates for the power oscillation period caused by momentary power supply oscillations.
2. Specified at 4.5 V for 5-V operation, and at 2.7 V for 3-V operation.
3. For if 4.5 V is not reached during 5-V operation, the internal reset circuit will not operate normally.
   In this case, the LSI must be initialized by software. (Refer to the Initializing by Instruction section.)

Figure 30 Internal Power Supply Reset